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TASK 5: GN&C PROCESSOR DEVELOPMENT and PFP INTEGRATION

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TASK 5: GN&C PROCESSOR DEVELOPMENT and PFP INTEGRATION

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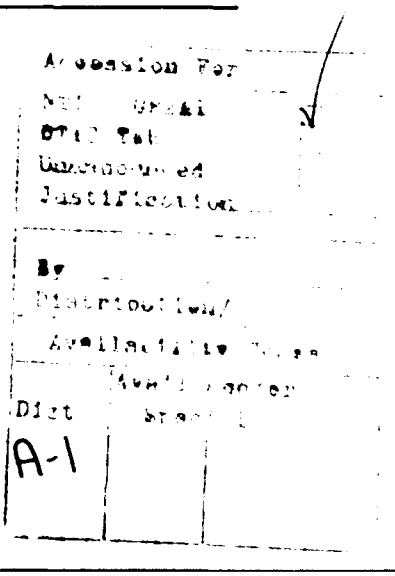

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1. Introduction

The Georgia Tech GN&C processor is being built from cutom designed VLSI chips, which have been designed at Georgia Tech. This volume covers the board level designs, system packaging, integration of a prototype into the Parallel Function Processor (PFP) environment for testing, and plans for using the PFP to test a radiation hardened version of the processor being built by Harris Corporation. Details on the design and test of the individual chips are covered in Volumes 6 and 7 of this report. In addition, this volume also covers the status of the currently available PFP systems, as well as their current functions and use, and plans for future PFP upgrades and improvements.

The simulation hardware in the DETL (the DETL facility is described in Volume 1 of this report) centers on the development, implementation, and use of the PFP. The PFP is a 64 processor digital computer for use in computationally intensive applications that can be partitioned into functional blocks. The processors are grouped in two 32 processor clusters running from one common host. Each 32 processor cluster is connected by a crossbar switch. All inter-processor communication takes place over the crossbar(s). Simultaneous transfers may take place independently and switch patterns may be changed every cycle. In order to program the machine correctly, all inter-processor communication and data transfer lengths must be known beforehand.

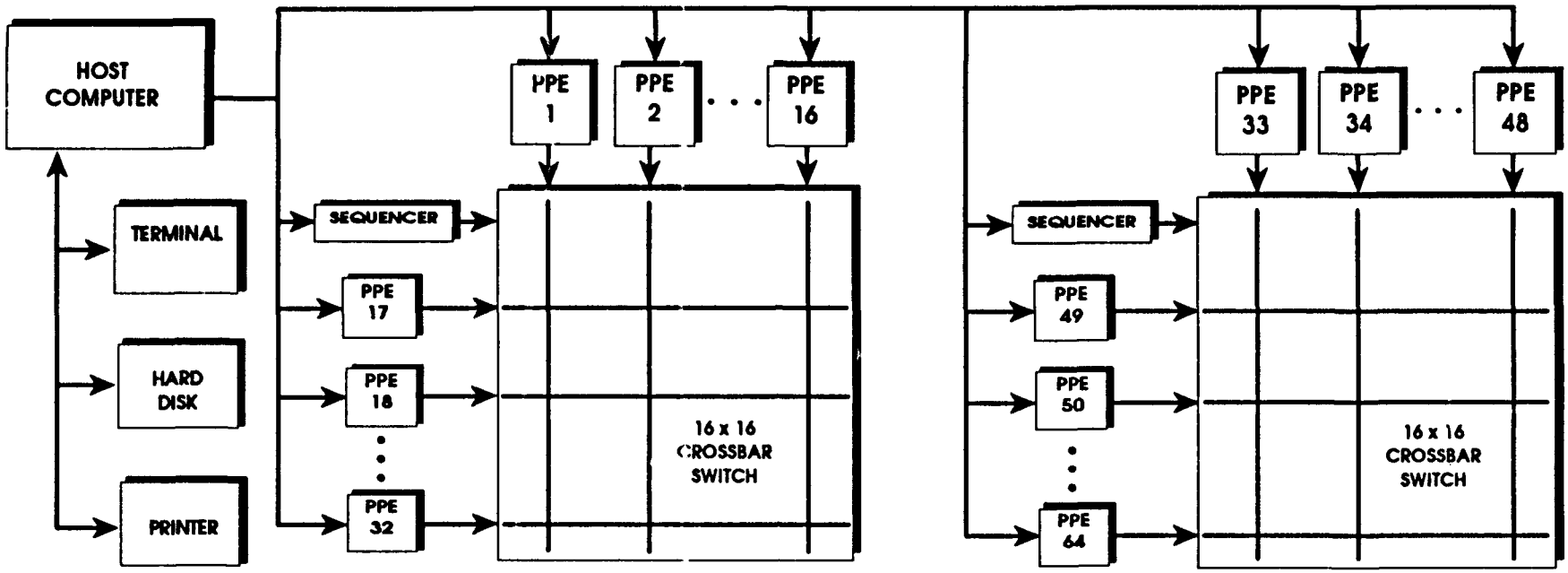
The PFP has been designed to support "hardware in the loop" simulations running in real time [1]. Actual hardware components may first be simulated on one or more processors and later replaced with actual hardware interfaced to specified crossbar ports. The inputs and outputs to/from the device will appear identical to those it would see in an actual system.

Figure 1.1 illustrates the basic PFP architectural concept. Figure 1.2 illustrates a front view of the actual machine. A deeper level of architectural detail can be found in the final report for FY89, volumes 1 and 2 [2], the final report for FY90, Volume 4 [3] , and in the PFP technical data package [4].

1.1. Objectives

Within DETL, there are two main hardware systems: The PFP and the Seeker Scene Emulator. The Seeker Scene Emulator is covered in Volume 2 of this report. The two systems are designed to function together as a simulation/emulation facility for kinetic energy weapons systems. The principal objectives of the DETL are as follows:

- Provide facilities for 6-DOF KEW emulation
- Provide real-time capability in excess of 2000 Hz
- Provide support for nonlinear functions
- Provide real-time emulation of IR FPA seekers
- Provide a facility for testing and verification of GN&C processors



HOST COMPUTER
- **SUN 386i**
  - FORTRAN
  - Ada
  - C
  - DIAGNOSTICS
  - UTILITIES
- **CROSSBAR**
  - TWO UNITS
  - 32 PORTS EACH
  - INTERCONNECTION BY ARI MODULE

PARALLEL PROCESSING ELEMENTS
- **64 NODES**
- **4 PROCESSOR TYPES**
  - INTEL ISBC 386/12
  - GT-FPP (32-BIT)
  - GT-FPX (64-BIT)
  - GT-I860
- **I/O A/D-D/A PPE**
  - SBX SERIAL PORT
  - SCSI
  - 1553

PERFORMANCE
- **GT-FPP**
  - 10 MFLOPS PEAK
- **GT-FPX**
  - 7.5 MFLOPS PEAK
- **ISBC 386/12**
  - 0.3 MFLOPS AVG.
- **DATA TRANSFERS**
  - 1.0 Gbps

Figure 1.1
Parallel Function Processor Architecture

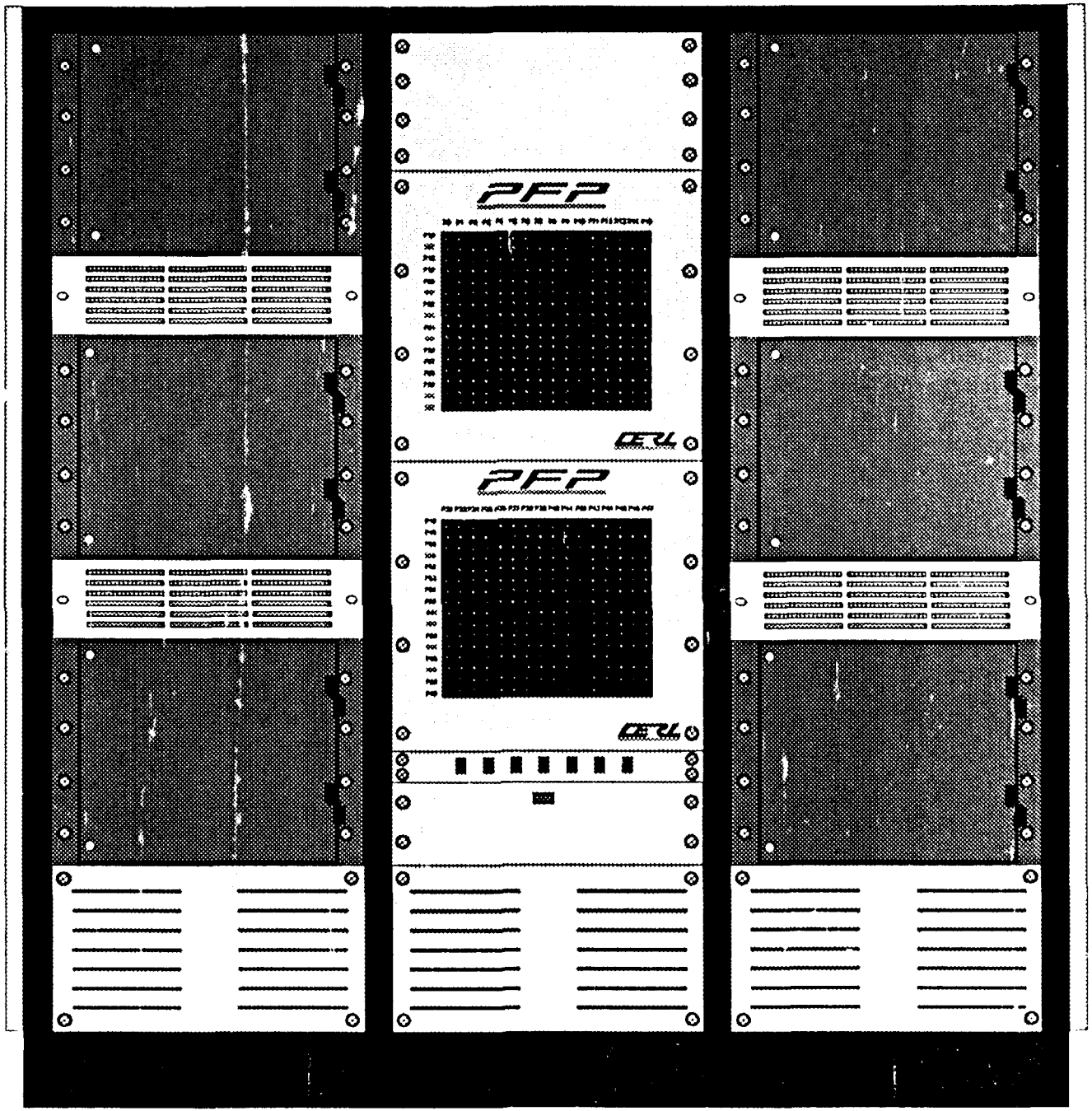


Figure 1.2

Parallel Processor (Front View)

Real-time emulation of IR FPA seekers is primarily the responsibility of the Seeker/Scene Emulator. The other objectives are primarily the responsibility of the PFP.

1.2. Requirements

The requirements for the period covered by this report fall into two main categories. The first category emphasizes using and supporting the PFP technology that has been developed for actual six degree of freedom (6-DOF) simulations and emulations, and integrated component testing.

The second category emphasizes the board and system level design, construction, integration, and testing of the Georgia Tech GN&C processor, which is built from custom IC's developed at Georgia Tech. A system packaging scheme has been developed, boards have been designed and built, and the boards have been and are being integrated into the PFP/SSE environment and tested. A third category, which is always under consideration is planned upgrades and improvements to the PFP systems.

The milestones met for the period covered by this report are as follows:

- Delivery and installation of a PFP unit to USADC/Huntsville's KDEC facility.
- A real time parallel Ada implementation of the EXOSIM V1.0 boost phase running on a PFP.
- A real time parallel C implementation of the EXOSIM V2.0 boost, mid-course and terminal phases running on a PFP.
- Design and construction of a prototype version of the Georgia Tech GN&C processor.
- Development of a stand alone PC hosted test station for the GN&C prototype.
- Integration and testing of the GN&C processor prototype in the PFP/SSE environment .

2. PFP

2.1 Existing PFP Systems and Their Use

The Digital Emulation Technology Laboratory has four in house PFPs currently in use and one PFP has been delivered to USADC's KDEC facility in Huntsville, Alabama. Two separate 32 processor system are located in the DETL's secure laboratory and have both been used extensively for classified work. A software development PFP, located outside the classified area, is primarily being used to develop and debug the software tools and operating environment that is eventually used to update the other PFP systems. This system is also used regularly for unclassified Ada development work. A fourth PFP system is available outside the classified area for testing and debugging new PFP boards.

Each of the four in house PFPs can be and are utilized in conjunction with or

independently of the other PFPs. For example, in the development of the multi-processor parallel implementation of the classified EXOSIM boost phase and the [classified EXOSIM] midcourse and terminal phases, a serial program was ported from a VAX environment to a single processor on the Intel 310 hosted thirty-two processor Intel 386 single board computer based PFP. The partitioning was then performed on the same PFP, and as each partition was finished it was moved to the Sun hosted thirty-two processor 386/FPP/FPX based PFP where the simulation was implemented and executed in real-time. The sixty-four processor Sun hosted software development system was being utilized for the implementation of the unclassified Ada version of the EXOSIM boost phase simulation, in addition to the continued development and refinement of the Sun host and FPP/FPX operations. The Sun hosted hardware development system is used for testing and debugging of new and existing hardware that is designated for the above mentioned PFPs.

The following five sections describe the configuration of each of the PFPs. Each section contains the current configurations and capabilities of the respective unit. The PFPs are configured as described, but on an as needed basis each or all of the parallel processing elements listed could be replaced with any of the other elements listed in Figure 1.

2.1.1 Intel 310 Hosted 80386 Based 32 Processor System

The Intel 310 hosted 80386 based 32 processor system is located in a secure area and is cleared for classified processing. The system hardware is configured with the following:

Host

- An 80386 Single Board Computer, 20 Mhz, 3 Mbytes RAM.
- Two 140 Mbyte removable hard disks.
- An HDS 200 terminal.

PFP

- One thirty-two port crossbar and sequencer combination.
- Twenty-four 20 MHZ Intel 80386 single board computers with 1 Mbyte RAM each.
- Eight 8 MHZ Intel 80286 single board computers with 1 Mbyte RAM each.

The system software is configured with the following :

Host

- C, FORTRAN, and Pascal compilers.

PFP

- C, FORTRAN, and Pascal compilers.

- Crossbar/Sequencer compiler.

- Processor, crossbar, and sequencer loaders.

- Ioserver - interface between the host and the processor.

This machine was heavily utilized in the partitioning of EXOSIM's boost phase, midcourse and terminal phases, and the end to end simulation. Since the machine is completely populated with commercially avaialable boards using commercially available compilers, the machine provides the most programming language choices of any of the in house PFPs. The off the shelf processors and compilers provide a wide range of capabilities for the user as parallel modules are designed and developed. This PFP has been used as the first platform in the process of bringing a serial program onto a PFP and beginning the parallel partitioning, because all of the serial programs obtained have been written in FORTRAN. The original code can be partitioned directly in FORTRAN, and re-compiled with the answers for each module verified directly against sections of the original code [5].

2.1.2 Sun Hosted FPP/FPX/80386 Based 32 Processor System

The Sun hosted FPP/FPX/80386 based 32 processor system is located in a secure area and is cleared for classified processing. The system hardware is configured with the following:

Host

- A 25 MHZ Sun 386i computer with 12 Mbytes RAM.

- Two 700 Mbyte SCSI removable hard disks.

- A 16 inch color Sun graphics monitor.

PFP

- One thirty-two port crossbar and sequencer combination.

- Twenty-two 10 MHZ, 8 Mflop GT-FPP single board computers.

- Six 8 MHZ, 6 Mflop, GT-FPX single board computers.

- Four 20 MHZ Intel 80386 single board computers with 1 Mbyte RAM each.

The system software is configured with the following:

Host

- C and FORTRAN compilers.

PFP

- C compilers for all 3 processor types.

- Ada-to-C and FORTRAN-to-C translators.

- The Crossbar/Sequencer compiler.

- Loaders for all processors, as well as the crossbar and sequencer.

- Software interface tools to allow for easy debug between the host and the processors.

This PFP was instrumental the implementation of EXOSIM's boost phase and midcourse terminal phases in real time. The Sun's graphic capabilities are put to use in the form of trajectory tracking and plotting. The interceptor and target are displayed in two planes in order to provide a good perspective of the missile's launch, stage separations, flip maneuver, midcourse diverts, target acquisition, frame rate changes, engagement diverts, and the interception. The implementation of this simulation also provides a testbed for the refinement of the C compilers for the GT-FPP and GT-FPX processors. This PFP is the second and final platform a simulation is ported to as the partitioning process progresses and the need for real time execution arises. Real time Ada implementations of classified simulations will be performed on this unit.

2.1.3 Sun Hosted FPP/FPX/80386 Based 64 Processor Software Development System

The Sun hosted FPP/FPX/80386 based 64 processor system is located outside of the secure area. The system is configured with the following hardware:

Host

- A 25 MHZ Sun 386i computer with 12 Mbytes RAM.

- A 700 Mbyte hard disk.

- A network interface.

- A 16 inch color Sun graphics monitor.

PFP

- Two thirty-two port crossbar and sequencer combinations (64 total crossbar ports).

- Eighteen 10 MHZ, 8Mflop GT-FPP single board computers.

- Six 8 MHZ, 6 Mflop GT-FPX single board computers.

The system software is configured with the following :

Host

- C and FORTRAN compilers.

PFP

- C compilers for all supported processors.

- Ada-to-C and FORTRAN-to-C translators.

- The Crossbar/Sequencer compiler.

- Loaders for the processors, crossbar, and sequencer.

- Software interface tools to allow for easy debug between the host and the processors.

This machine is used regularly for simulations [6] and was instrumental in the real-time implementation of the unclassified EXOSIM boost phase simulation in both FORTRAN and Ada. The graphic capabilities are put to use in the form of trajectory tracking and plotting. As with the previous PFP system, this machine is used in the refinement of the C compilers for the GT-FPP and GT-FPX processors, along with the development of new capabilities for the Sun hosted systems. The development, execution, and refinement of the Ada modules are performed on this machine.

2.1.4 Sun Hosted Hardware Development System

The Sun hosted hardware development system is located outside of the secure area. The system hardware is configured from the following:

Host

- A 25 MHZ Sun 386i computer with 12 Mbytes RAM.

- A 300 Mbyte hard disk.

- A network interface.

- A 16 inch color Sun graphics monitor.

PFP

- One thirty-two port crossbar and sequencer combination.

- Twenty-five 10 MHZ, 8 Mflop GT-FPP single board computers.

The system software consists of the following :

Host

- C and FORTRAN compilers.

PFP

- C compilers for both the GT-FPP and GT-FPX processors.

- A FORTRAN-to-C translator.

- The Crossbar/Sequencer compiler.

- Loaders for the processors, crossbar, and sequencer.

- Software interface tools to allow for easy debug between the host and the processors.

This machine is used as a hardware testbed to support for the Sun hosted PFPs. Starting with the original diagnostics written on the Intel 310 systems, Sun based diagnostics to test the integrity of the multibus paths between the host and (i) the processors and (ii) the crossbar and sequencer combinations have been developed. In addition to this, two other test programs were written to test the crossbar, sequencer, and processor interconnections. The first verifies the processor to sequencer handshake lines and performs a minimal check on the crossbar data paths. The second performs a rigorous confidence test on the whole thirty-two port crossbar network, with the main concentration on the reliability of the data transfers between any single port and all other ports. After development, the applicable diagnostics can be moved to the other Sun based systems as needed.

2.1.5 KDEC System

The KDEC system is located at USADC's KDEC facility in Huntsville Alabama. The system is hosted by Intel 310 and consists of the following hardware configuration:

Host

- An 8 MHZ 80286 based Intel 310 computer with 3 Mbytes RAM.

- A 140 Mbyte hard disk.

- An HDS 200 terminal.

- A 2400 baud modem.

PFP

- One thirty-two port crossbar and sequencer combination.

- Thirty-two 8 MHZ Intel 80286 single board computers with 1 Mbyte RAM each.

The system software consists of the following :

Host

- C, FORTRAN, and Pascal compilers.

PFP

- C, FORTRAN, and Pascal compilers.

- The Crossbar/Sequencer compiler.

- Loaders for the processors, crossbar, and sequencer.

- Interface programs between the host and the processors to aid in debug.

This machine was utilized in the partitioning of the unclassified version of FXOSIM's boost phase simulation and is now in the located in the Simulation Center at the KDEC facility in Huntsville, Alabama. A training course for several users was conducted in Huntsville and this machine was utilized during the laboratory time. Several simulations developed at DETL have been delivered to the KDEC facility and have been installed on the machine. Users work with the machine on a weekly basis using these simulations.

This PFP has the capability of supporting sixty-four parallel processing elements, with two thirty-two port crossbar networks and the two companion sequencers. The current configuration consists, as noted above, of only one crossbar and sequencer combination and thirty-two 80286 processors. This configuration was delivered to provide a solid, proven environment for the KDEC programmers to learn the system. Plans have been delivered to upgrade the PFP including replacement of the host, upgrading to higher performance processors, and the possible installation of a dynamically reconfigurable crossbar switch. Georgia Tech provides system support for this PFP, along with delivering unclassified and classified parallel simulations to KDEC facility.

3. GN&C Processor Development

3.1. The Georgia Tech GN&C Processor Board and System Development

The architecture of the Georgia Tech GN&C Processor is shown in Figure 3.1. The architecture consists of up to eight processors connected by a crossbar switch. Two types of processors have been designed, called the Data Processor and the Executive Processor, respectively. The Data Processor is used for tight control loops that require small memory. It is built from four custom VLSI chips and has no external memory. The Executive Processor consists of four custom VLSI chips plus external memory for data and instructions. This processor can serve as an I/O processor and an object processor.

In addition, a Signal Processor consisting of six custom VLSI chips is included in the package. The functions included in the SP chain are spatial filtering, temporal filtering, non-uniformity compensation, thresholding, clustering, and centroiding. Details on the functionality of each of these custom chips, including the Executive and Data Processors, can be found in Volume 7 of this report.

The physical construction of the processor package consists of a collection of stackable modules, which are shown in Figure 3.2. Since the system is modular, different combinations of

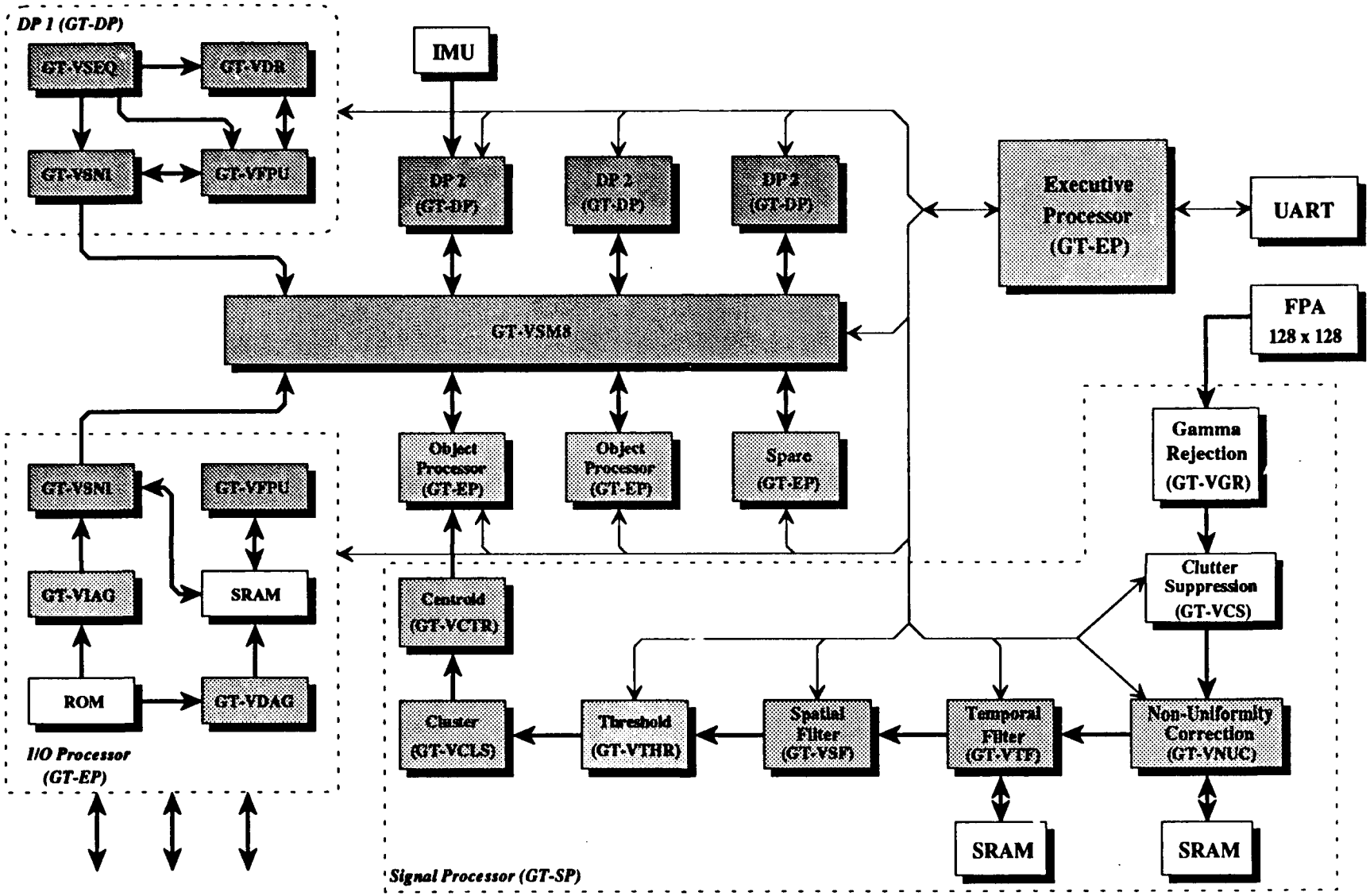


Figure 3.1
Georgia Tech GN&C Processor Architecture

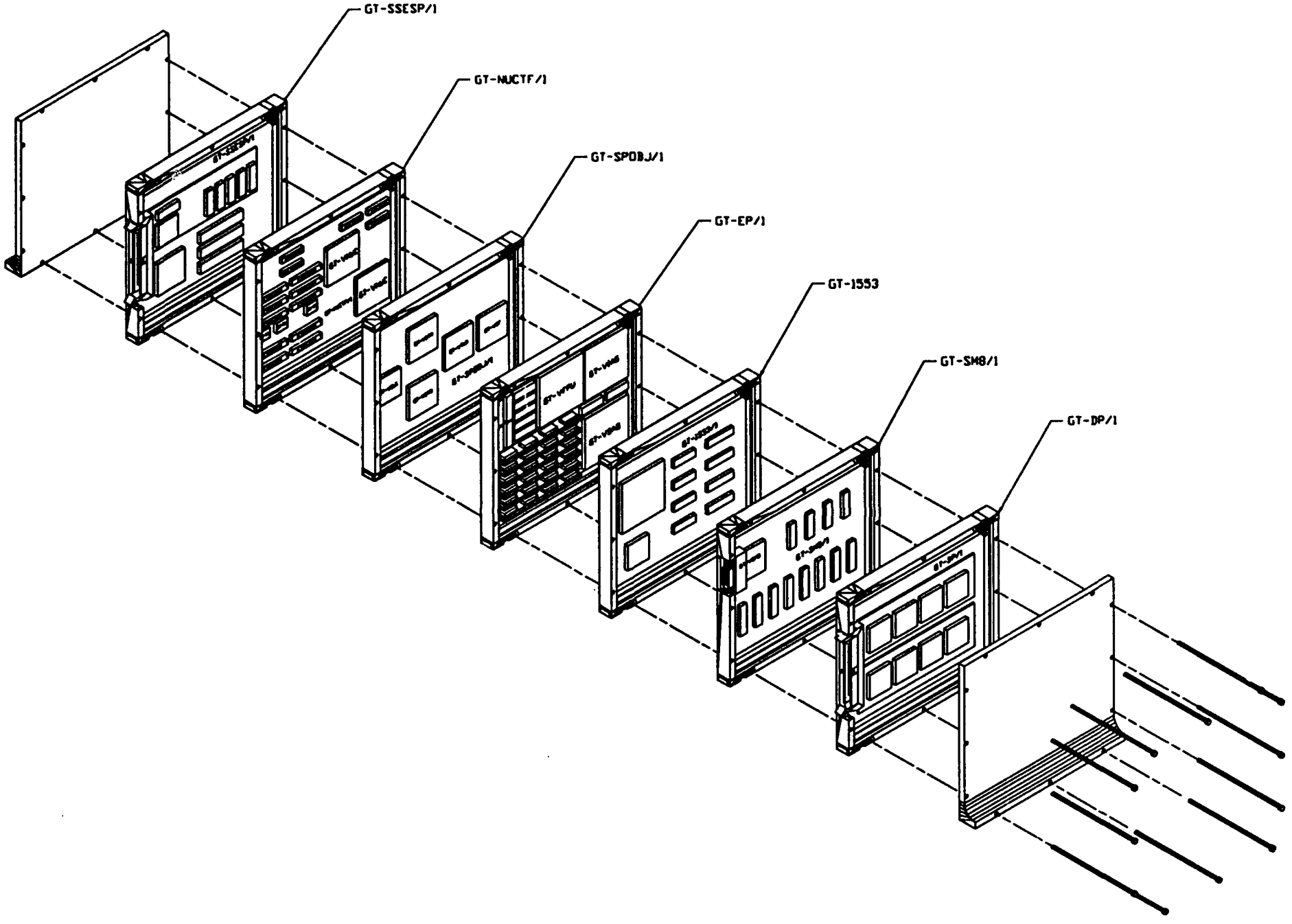


FIGURE 3.2
GN$C SYSTEM CONFIGURED WITH 2 DATA PROCESSORS

modules can be put together to configure a system for a specific application. Figure 3.2 illustrates a configuration with one Executive Processor and two Data Processors. Figure 3.3 shows a configuration with one Executive processor and six Data Processors. The computing requirements for the particular application will dictate which modules are included in the stack. Other configurations, for example omitting the signal processing or 1553 portions, or adding new functions, are arrived at in a similar building block type manner.

The physical size of the boards in the system is 5.90" by 6.65". This format is identical to the size of the boards in the Honeywell S5 flight processor, but the signal definitions and circuitry are all based on the Georgia Tech GN&C chip set. Each board contains four rows of 63 pin stackable connectors, which are used make the electrical connections between modules. Two of these connectors, J1 and J2, are permanently dedicated to the EP bus, which serves as the master bus running throughout the stack. The other two connectors, J3 and J4, are dedicated to the SP bus on the signal processing boards. This bus carries all of the communication needed between the signal processing modules, which can happen concurrently with activity on the EP bus. The last SP board in the stack does not pass the SP signals to the other modules in the stack. Only the power, grounds, and system clocks are passed to the non SP boards so that the unused pins on these two connectors are available for other assignments as needed. New modules can be designed and added to the stack by meeting these standard bus specifications.

The Georgia Tech GN&C Processor Prototype structure is shown in a closed configuration in Figure 3.4. External connections include the 1553 bus, RS-422 lines, a PFP crossbar port, a high speed serial port, and a seeker interface port. The 1553 bus and RS-422 lines have been added to provide the same interfaces needed for the AHAT processor, which is to be tested at the DETL. External devices will generate the same signals and input them in the same way. Internally the AHAT configuration will be based on the same chip designs, but the chips will be radiation hardened versions in a Harris devised packaging scheme. It will use the 1553 bus as its main source or communication, and accept interrupts from internal or external devices, generate interrupts or signals for internal devices and manage all the incoming and outgoing traffic. All external interrupts will be sent through the differential RS-422 channels.

The prototype design is based on the Honeywell S-5 form factor. The internal signal bus has been changed to support the Georgia Tech architecture.The EP bus definitions for connectrs J1 and J2 are given in Tables 1 and 2 respectively. The SP bus definitions for connectors J3 and J4 are given in Tables 3 and 4 respectively.

3.1.1 The GT-SSESP/1

The GT-SSESP/1, which is currently in the fabrication stage, will serve two purposes. First, it will serve as the external interface between the seeker hardware and the GN&C's signal processor in the processor's actual flight configuration. Second, all system clocks, including the EP bus host clock, the pixel clock, and the non-uniformity compensation clock, will be generated on this board. Both the pixel clock and non-uniformity compensation clock will be programmable from the host processor. The seeker interface consists of a 16 bit parallel data interface, the pixel clock (which the pixel data must synchronized to), and four other synchronizing signals. These four signals, called begin frame, begin row, end frame, and end

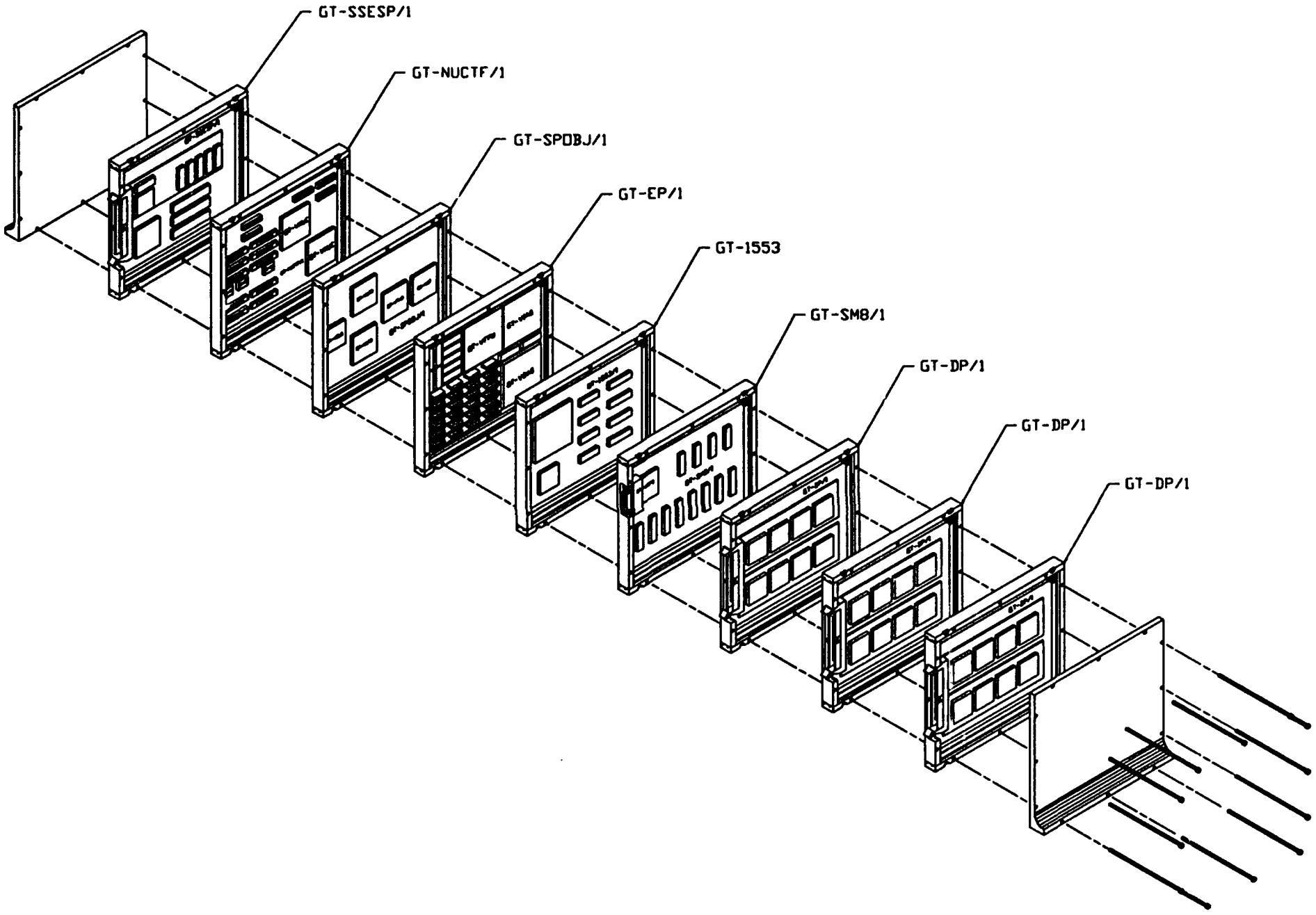
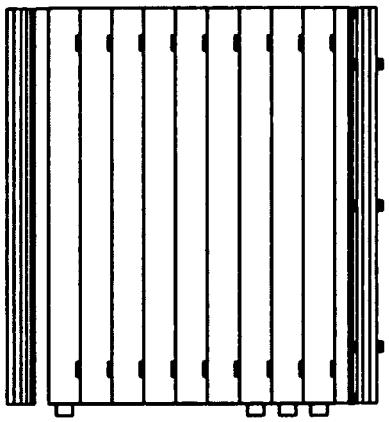
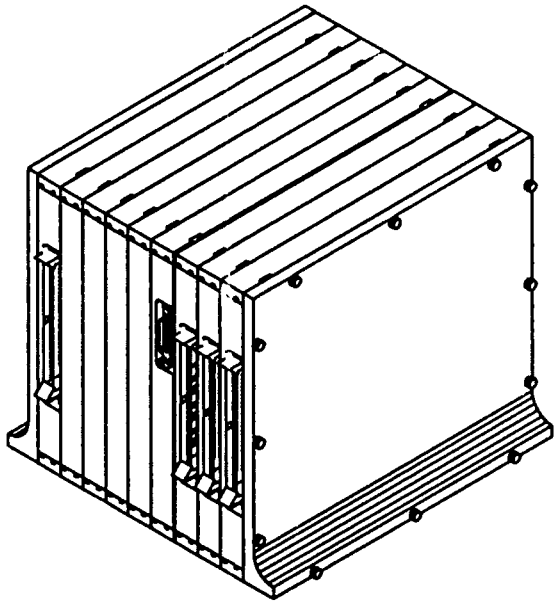


FIGURE 3.3

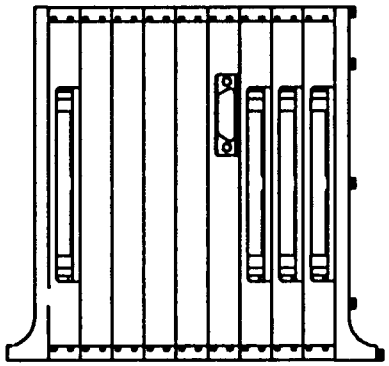
GN$C SYSTEM CONFIGURED WITH SIX DATA PROCESSORS



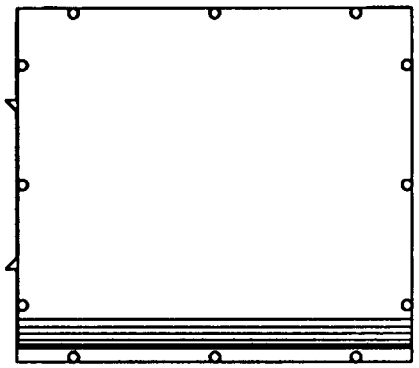
TOP VIEW



ISOMETRIC VIEW



FRONT VIEW



RIGHT VIEW

FIGURE 3.4
GN$C SYSTEM IN CLOSED FORM

TABLE 1

Definition of EP Bus Signals on the J1 Connector

Connector	EP BUS Pin Number	Signal Name
J1	Pin 1	+5V
J1	Pin 2	GND
J1	Pin 3	+5V
J1	Pin 4	GND
J1	Pin 5	+5V
J1	Pin 6	GND
J1	Pin 7	HADR_0
J1	Pin 8	HADR_1
J1	Pin 9	HADR_2
J1	Pin 10	HADR_3
J1	Pin 11	HADR_4
J1	Pin 12	HADR_5
J1	Pin 13	HADR_6
J1	Pin 14	HADR_7
J1	Pin 15	HADR_8
J1	Pin 16	HADR_9
J1	Pin 17	HADR_10
J1	Pin 18	HADR_11
J1	Pin 19	HADR_12
J1	Pin 20	HADR_13
J1	Pin 21	HADR_14
J1	Pin 22	HADR_15
J1	Pin 23	HADR_16
J1	Pin 24	HADR_17
J1	Pin 25	HADR_18
J1	Pin 26	HADR_19
J1	Pin 27	HADR_20
J1	Pin 28	HADR_21
J1	Pin 29	+5V
J1	Pin 30	GND
J1	Pin 31	+5V

TABLE 1 (continued)

Definition of EP Bus Signals on the J1 Connector

J1	Pin 32	GND
J1	Pin 33	+5V
J1	Pin 34	GND
J1	Pin 35	HADR_22
J1	Pin 36	HADR_23
J1	Pin 37	HADR_24
J1	Pin 38	HADR_25
J1	Pin 39	DAV2
J1	Pin 40	DAV3
J1	Pin 41	INT_0
J1	Pin 42	INT_1
J1	Pin 43	INT_2
J1	Pin 44	INT_3
J1	Pin 45	INT_4
J1	Pin 46	INT_5
J1	Pin 47	INT_6
J1	Pin 48	INT_7
J1	Pin 49	INT_8
J1	Pin 50	STATUS_0
J1	Pin 51	STATUS_1
J1	Pin 52	STATUS_2
J1	Pin 53	STATUS_3
J1	Pin 54	STATUS_4
J1	Pin 55	READ2
J1	Pin 56	READ3
J1	Pin 57	RESET
J1	Pin 58	IOS
J1	Pin 59	+5V
J1	Pin 60	GND
J1	Pin 61	+5V
J1	Pin 62	GND
J1	Pin 63	+5V

TABLE 2

Definition of EP Bus Signals on the J2 Connector

Connector	EP BUS Pin Number	Signal Name
J2	Pin 1	+5V
J2	Pin 2	GND
J2	Pin 3	+5V
J2	Pin 4	GND
J2	Pin 5	+5V
J2	Pin 6	GND
J2	Pin 7	DATA_0
J2	Pin 8	DATA_1
J2	Pin 9	DATA_2
J2	Pin 10	DATA_3
J2	Pin 11	DATA_4
J2	Pin 12	DATA_5
J2	Pin 13	DATA_6
J2	Pin 14	DATA_7
J2	Pin 15	DATA_8
J2	Pin 16	DATA_9
J2	Pin 17	DATA_10
J2	Pin 18	DATA_11
J2	Pin 19	DATA_12
J2	Pin 20	DATA_13
J2	Pin 21	DATA_14
J2	Pin 22	DATA_15
J2	Pin 23	DATA_16
J2	Pin 24	DATA_17
J2	Pin 25	DATA_18
J2	Pin 26	DATA_19
J2	Pin 27	DATA_20
J2	Pin 28	DATA_21
J2	Pin 29	DATA_22
J2	Pin 30	GND
J2	Pin 31	+5V

TABLE 2 (continued)

Definition of EP Bus Signals on the J2 Connector

J2	Pin 32	GND
J2	Pin 33	+5V
J2	Pin 34	DATA_23
J2	Pin 35	DATA_24
J2	Pin 36	DATA_25
J2	Pin 37	DATA_26
J2	Pin 38	DATA_27
J2	Pin 39	DATA_28
J2	Pin 40	DATA_29
J2	Pin 41	DATA_30
J2	Pin 42	DATA_31
J2	Pin 43	DS_0
J2	Pin 44	DS_1
J2	Pin 45	DS_2
J2	Pin 46	DS_3
J2	Pin 47	NCS2
J2	Pin 48	NCS3
J2	Pin 49	RFI2
J2	Pin 50	RFI3
J2	Pin 51	0DSSEL
J2	Pin 52	IDSSEL
J2	Pin 53	WRITE2
J2	Pin 54	WRITE3
J2	Pin 55	DR
J2	Pin 56	GND
J2	Pin 57	HST_CLK
J2	Pin 58	GND
J2	Pin 59	PXL_CLK
J2	Pin 60	GND
J2	Pin 61	+5V
J2	Pin 62	GND
J2	Pin 63	+5V

TABLE 3

Definition of SP Bus Signals on the J3 Connector

Connector	SP BUS Pin Number	Signal Name
J3	Pin 1	+5V
J3	Pin 2	GND
J3	Pin 3	+5V
J3	Pin 4	GND
J3	Pin 5	+5V
J3	Pin 6	GND
J3	Pin 7	SF_IN0
J3	Pin 8	SF_IN1
J3	Pin 9	SF_IN2
J3	Pin 10	SF_IN3
J3	Pin 11	SF_IN4
J3	Pin 12	SF_IN5
J3	Pin 13	SF_IN6
J3	Pin 14	SF_IN7
J3	Pin 15	SF_IN8
J3	Pin 16	SF_IN9
J3	Pin 17	SF_IN10
J3	Pin 18	SF_IN11
J3	Pin 19	SF_IN12
J3	Pin 20	SF_IN13
J3	Pin 21	SF_IN14
J3	Pin 22	SF_IN15
J3	Pin 23	SF_BFR_I
J3	Pin 24	SF_BRW_I
J3	Pin 25	SF_EFR_I
J3	Pin 26	SF_ERW_I
J3	Pin 27	No Connection
J3	Pin 28	No Connection
J3	Pin 29	+5V
J3	Pin 30	GND
J3	Pin 31	+5V

TABLE 3 (continued)

Definition of SP Bus Signals on the J3 Connector

J3	Pin 32	GND
J3	Pin 33	+5V
J3	Pin 34	GND
J3	Pin 35	PXL_CLK
J3	Pin 36	GND
J3	Pin 37	No Connection
J3	Pin 38	No Connection
J3	Pin 39	No Connection
J3	Pin 40	No Connection
J3	Pin 41	No Connection
J3	Pin 42	No Connection
J3	Pin 43	No Connection
J3	Pin 44	No Connection
J3	Pin 45	No Connection
J3	Pin 46	No Connection
J3	Pin 47	No Connection
J3	Pin 48	No Connection
J3	Pin 49	No Connection
J3	Pin 50	No Connection
J3	Pin 51	No Connection
J3	Pin 52	No Connection
J3	Pin 53	No Connection
J3	Pin 54	No Connection
J3	Pin 55	No Connection
J3	Pin 56	No Connection
J3	Pin 57	No Connection
J3	Pin 58	No Connection
J3	Pin 59	No Connection
J3	Pin 60	No Connection
J3	Pin 61	No Connection
J3	Pin 62	No Connection
J3	Pin 63	No Connection

TABLE 4

Definition of SP Bus Signals on the J4 Connector

Connector	SP BUS Pin Number	Signal Name
J4	Pin 1	+5V
J4	Pin 2	GND
J4	Pin 3	+5V
J4	Pin 4	GND
J4	Pin 5	+5V
J4	Pin 6	GND
J4	Pin 7	NUC_IN0
J4	Pin 8	NUC_IN1
J4	Pin 9	NUC_IN2
J4	Pin 10	NUC_IN3
J4	Pin 11	NUC_IN4
J4	Pin 12	NUC_IN5
J4	Pin 13	NUC_IN6
J4	Pin 14	NUC_IN7
J4	Pin 15	NUC_IN8
J4	Pin 16	NUC_IN9
J4	Pin 17	NUC_IN10
J4	Pin 18	NUC_IN11
J4	Pin 19	NUC_IN12
J4	Pin 20	NUC_IN13
J4	Pin 21	NUC_IN14
J4	Pin 22	NUC_IN15
J4	Pin 23	NUC_BFR_I
J4	Pin 24	NU_BRW_I
J4	Pin 25	NU_EFR_I
J4	Pin 26	NU_ERW_I
J4	Pin 27	No Connection
J4	Pin 28	No Connection
J4	Pin 29	+5V
J4	Pin 30	GND
J4	Pin 31	+5V

TABLE 4 (continued)

Definition of SP Bus Signals on the J4 Connector

J4	Pin 32	GND
J4	Pin 33	+5V
J4	Pin 34	GND
J4	Pin 35	PXL_CLK
J4	Pin 36	GND
J4	Pin 37	No Connection
J4	Pin 38	No Connection
J4	Pin 39	GND
J4	Pin 40	GND
J4	Pin 41	GND
J4	Pin 42	GND
J4	Pin 43	+5V
J4	Pin 44	GND
J4	Pin 45	+5V
J4	Pin 46	GND
J4	Pin 47	+5V
J4	Pin 48	GND
J4	Pin 49	+5V
J4	Pin 50	GND
J4	Pin 51	+5V
J4	Pin 52	GND
J4	Pin 53	+5V
J4	Pin 54	GND
J4	Pin 55	+5V
J4	Pin 56	GND
J4	Pin 57	+5V
J4	Pin 58	GND
J4	Pin 59	+5V
J4	Pin 60	GND
J4	Pin 61	+5V
J4	Pin 62	GND
J4	Pin 63	+5V

row, are generated by the seeker hardware, are based on the size of the focal plane array, and are also synchonized to the pixel clock. Schematics for the GT-SSESP/1 are included in Appendix A. Details on the interface timing are provided in Volume 6 of this report. For testing in the DETL, Georgia Tech's Seeker Scene Emulator will be used to input the seeker data to this port.

3.1.2 The GT-NUCTF/1

The GT-NUCTF/1 board contains the circuitry for the non-uniformity compensation and temporal filtering functions as well as the external memory that each requires (128 kilobytes is required by temporal filtering and 192 kilobytes is required by the non-uniformity compensation). The board design is complete and the board is currently in fabrication. The board contains both an EP bus interface and an SP bus interface. Filter coefficients are loaded over the host EP bus, and buffered pixel data is fed from the GT-SSESP/1 over the SP bus into the non-uniformity compensation chip. The pixel stream then enters the temporal filter, with the filtered pixel stream exiting the board through the SP bus. Schematics for the GT-NUCTF/1 are included in Adppendix A.

3.1.3 The GT-SPOBJ/1

The GT-SPOBJ/1 contains the spatial filtering, thresholding, clustering and centroiding functions. The board has been fabricated, tested, and used in actual closed loop demonstrations. Filter coefficients are loaded over the host EP bus. The pixel data stream enters the board from the SP bus after already passing through the non-uniformity compensation and temporal filtering functions. The data stream then passes through spatial filtering, thresholding, clustering, and centrioding, respectively. The centroided object information can then be read by the object processor over the EP bus. Schematics for the GT-SPOBJ/1 are included in Appendix A.

3.1.4 The GT-EP1553/1

The GT-1553/1 board contains the 1553 bus and RS-422 interfaces needed to match the functionality of the Harris AHAT processor. The board is at the end of the design phase and ready to move into fabrication. The 1553 bus interface, can be configured to act as a bus master or slave and appears as a device connected to the host EP bus. The RS-422 lines are used to provide processor interrupts from external sources which are translated on board, and sent to the processor over the EP bus.

3.1.5 The GT-SM8/1

The SM8 Module is built around a custom VLSI crossbar switch chip that has eight processor ports. Figure 2.1 allocates one to the Executive Processor Module, two to the Data Processor Module, and one to the Object Processor Module. A full configuration would add an additional Data Processor Module and two Object Processor Modules as shown in Figure 3.4. These could be swapped depending on requirements.

A high speed serial port and a PFP crossbar port are also provided on the SM8 module. The high speed port connects directly to the EP bus which is used to load the SM8 and the DP. The crossbar port can be used to connect the GN&C processor directly to a PFP unit, so that the

system simply appears as another node.

Initially the Georgia Tech prototype was to contain no 1553 bus. However, since Georgia Tech plans to test the AHAT processor, it was felt a 1553 bus interface was needed to make sure we had this capability in our test program. Since the GT internal architecture is not identical to AHAT, it was decided to design our own I/O interface chip and base it on one or two FPGAs. This would permit us to use a fast turnaround on our design with complete control of the design and implementation program. Also, since the board has been designed as a stand alone module it can be omitted when no longer needed.

3.1.6 The GT-S5EP/1

The GT-S5EP/1 is built from Georgia Tech's Executive Processor Chip set, consisting of 4 custom VLSI chips and external memory. The board can serve as the executive, or master processor in the system, an object processor, or any other computationally intensive function that requires a larger memory than a DP module can handle. Details on the EP chip set can be found in Volume 7 of this report.

An EP evaluation board has been built and is currently in testing. The GN&C module will contain the same circuitry, but require a new board layout and some modifications to meet the module format. The GN&C module layout will be completed as soon as the evaluation board has been fully tested.

3.1.7 The GT-S5DP/1

The GT-S5DP/1 is capable of supporting two data processing modules, each with an interface to the EP bus and each with an interface to the SM8 switch. Each DP is configured using four custom VLSI chips mounted on a daughter board. The daughter boards are then mounted to the base module. The DP modules are used for jobs requiring tight control loops and moderate memory requirements. Details on the DP chip set can be found in Volume 7 of this report.

A prototype S5DP board consisting of one DP daughter board and a crossbar interface has been built, integrated into the module stack, tested, and used in laboratory demonstrations. Schematics of this prototype are provided in Appendix A. The printed circuit version of the base module is in the design phase.

3.1.8 The GT-SPAT/1 and GT-GNCTST/1

The GT-SPAT/1 and GT-GNCTST/1 are a board set that allow a standard IBM AT or compatible machine to interface to the GN&C processor's EP bus and act as the bus master. The GT-SPAT/1 board is an AT add in board that resides inside the AT host, while the GT-GNCTST/1 plugs into the modular GN&C stack. All relevant EP bus signals are passed through a set of six 34 pin ribbon cables between the two boards. In addition, the GT-GNCTST/1 also contains an interface to the Seeker Scene Emulator for inputting pixel data to the SP boards. The the GT-SPAT/1 board has been designed so that it can work anywhere in the host AT's I/O space by setting the right DIP switch combinations, but it is reccomended that the board be set to

operate on the 300h to 31Fh I/O space. (This space has been set aside in the AT reference manual for prototype hardware, so possible overlap with other boards in the system can be minimized.) The board uses a total of 7 ports that serve to control and/or monitor various functions in the GN&C package. Schematics for both the GT-SPAT/1 and GT-GNCTST/1 are included in Appendix A.

The interface to the processor is established directly through an EP bus interface. All data, address, and control lines that are usually driven by the GT-S5EP/1 board are connected. Since there is a very large number of application programs and programming languages available for the AT, it can serve as a very flexible test station, and as a software development platform. While AT class machines do not run anywhere near the speeds of the Georgia Tech EP chip set, a large amount of functional testing has been accomplished using this configuration.

The GT-SPAT/1 interface is designed to communicate with all EP data, address, and status bits through data ports in the AT's I/O space. The EP data bus is designed for 32 bit data transfers, has 26 bits of address capability, requires monitoring of 18 status lines, and requires 15 control bits. The AT data bus is designed for 16 bit data transfers. The interface has been built so that these functions are divided over 7 separate I/O ports. The 32 bit data bus is divided among two 16 bit ports. The 26 bit address bus is divided among two 16 bit ports. The 18 status bits are divided among two 16 bit ports and the 15 control bits are set up as one port. Table 5 lists the port assignments and their respective addresses.

Table 5. GT-SPAT/1 Port Assignments

ADDRESS BIT	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	HEX
CONTROL WORD	1	1	0	0	0	0	0	0	0	0	0300
LOW DATA	1	1	0	0	0	0	0	0	1	0	0302
HIGH DATA	1	1	0	0	0	0	0	1	0	0	0304
LOW ADDRESS	1	1	0	0	0	0	0	1	1	0	0306
HIGH ADDRESS	1	1	0	0	0	0	1	0	0	0	0308
LOW STATUS	1	1	0	0	0	0	1	0	1	0	030A
HIGH STATUS	1	1	0	0	0	0	1	1	0	0	030C

Details on individual bit assignments within each I/O port are available in the GT-SPAT/1 reference manual. The functionality of each bit in each port is described, as well as the mapping of what bit that function has been assigned to.

3.1.9 The GT-VDSTST/1

The GT-VDSTST/1 (Video Data Stream TeST) has been designed to allow functional testing of the SP modules without requiring a seeker input. The board has been built and tested, and is currently use. The board consists of an EP bus interface, a 64K by 16 memory, a counter that generates memory addresses as well as the begin frame, begin row, end frame, and end row signals, clock generation circuitry, and an SP bus interface. The board can be inserted in the module stack in place of the GT-SSESP/1 and seeker, and be used to simulate seeker input. Four frames of 128 by 128 seeker data can be loaded into the board's memory by the host or executive processor over the EP bus. The counter circuitry is then activated by the host and the four frames are sent out repetitively until the counter is disabled. Scematics for the GT-VDSTST/1 are included in Appendix A.

The GT-VDSTST/1 eliminates the need for an external seeker input for functional testing, thus reducing the amount of test equipment needed and simplifying the programming effort. Once the the SP hardware has been funtionally verified, it can be tested at full speed with a complete image using the Seeker Scene Emulator.

Two sets of EP bus lines, the device select lines and address lines, are used to access the circuitry on the VDSTST board. Four device select lines, DS0 through DS4, are used to select the board. These lines asserted by the host must match an on board setting, which is programmed in an on board EPLD. The board is currently set as device number 4, but can be changed at any time by reprogramming the EP bus interface EPLD located in socket U6.

There are two modes of operation on the VDSTST, the load mode and run mode, which are selected by writing to a control bit. The control bit is located at data bit 0, of address 0x10000 when device 4 is selected. Setting the control bit to 0 puts the board on load mode, which allows the host to read and/or write any memory location on the board. Setting the control bit to 1 activates the on board address counter and enables the pixel data output on the SP bus. The control bit may be read or written at any time.

The VDSTST memory is sequentially accessed, as 16 bit words, from addresses 0x0000 through 0xFFFF when device 4 is selected and the board is in load mode. Any memory location can be read or written in any Table 6 lists the complete address map for the board:

Table 6. GT-VDSTST Memory Map

Function	DS3	DS2	DS1	DS0	Address A0-A15
Control Bit (*)	0	1	0	0	0x10000
Memory	0	1	0	0	0x00000 - 0x0FFFF

(*) Control Bit is D0 of data word. Control bit is set to 0 for load mode. Control bit is set to 1 for run mode.

Four frames of 128 by 128 image data are loaded into a 64k deep memory as 16 bit words. The frame is loaded sequentially by rows, with the first pixel of the first frame loaded to address 0x00001 and the last pixel of the first frame loaded at 0x04000. The other three frames are loaded similarly, as shown in Table 7. Frame 4 has one minor exception. The begin frame pulse, which occurs on an all 0 count from the address generation counter for frame 1, must occur one pixel clock cycle before the first pixel data. This causes the data skew so that the first pixel is loaded to location 0x00001 instead of location 0x00000, with the result being that the last pixel is "wrapped around" and loaded at location 0x00000.

Table 7. Frame Load Addressing

Frame Number	Starting Pixel Address	Ending Pixel Address
1	0x0001	0x4000
2	0x4001	0x8000
3	0x8001	0xC000
4	0xC000	0x0000

3.1.10 Stand Alone Testing

Using the GT-VDSTST/1, GT-SPAT/1, and GT-GNCTST/1 and an IBM AT or AT compatible machine as a host, a stand alone test facility exists for module development, debug, and testing which is outside of the DETL secure area. Focal Plane Array test patterns can be generated and loaded into the VDSTST board, processed through the SP modules, DP modules, and EP modules. This alternative testing ability allows new boards to be tested and debugged, and new software algorithms developed, while working boards are available for use in the closed loop simulation and testing.

4. PFP/GN&C/SSE Integration for Emulation and Testing

As stated in the introduction, the primary purpose of the DETL facility is for

simulation/emulation and hardware in the loop testing. A six degree of freedom simulation called EXOSIM, described in detail in Volume 3 of this report, has been implemented on the PFP and served as the base for a hardware in the loop demonstration.

4.1 EXOSIM Closed Loop Demonstration

The EXOSIM closed loop demonstration showcased the PFP and SSE systems' abilities as real time test equipment, with the prototype GN&C processor as the article under test. The EXOSIM engagement contains an interceptor with a staring array seeker and one or more objects in the threat. Real time emulation is possible without special purpose seeker hardware if a simple seeker is modeled and only one or two objects are used. For a real staring array and multiple objects, the processing demands are too large for the processors currentlt used in the PFP , thus requiring the use of the SSE. Interfaces were developed and implemented so that the SSE fed image data directly into the GN&C processor, and so the GN&C processor could send object data directly to the PFP for tracking. Figure 3.5 illustrates the configuration that was used and the interfaces that were developed.

5. New Developments

5.1 Support for Other Programs

5.1.1 AHAT Testing

Preliminary plans are to bring a Harris built radiation hardened processor based on the Georgia Tech GN&C chip set (the AHAT processor), to the DETL for testing. The Harris AHAT GN&C Processor and the Georgia Tech processor will have the same interfaces and are functionally similar. The AHAT Processor contains 3 EPs, SM8, SP, Gris Gamma rejection, 1553 interface, IOS, RS-422 discrete I/Os and memory.

Harris plans to use the 1553 bus for all external I/O programming on AHAT. All devices external to the processor will interface to the 1553 bus through isolation transformers. The 1553 inside the processor is controlled by a bus master. For any external device to send data to the processor requires an interrupt which will generate a read by the processor on a particular device such as the IMU. Other interrupts, such as end-of-row or end-of-frame are generated by the FPA. All of these interrupt and signal lines are passed over the RS-422 bus.

Internal to the processor, Harris has developed a custom I/O chip to resolve the data traffic issues. The I/O chip maps all of the 1553 structure into the EP memory. The EP can then be programmed to sort and distribute the incoming data and to send out data with the correct destination address.

Discrete events generated by external signals will use the RS-422 bus. Most will terminate at the EP, but some will go to the 1553 I/O interface. Discrete outputs will be generated by the EP and sent over the RS-422 bus to external devices.

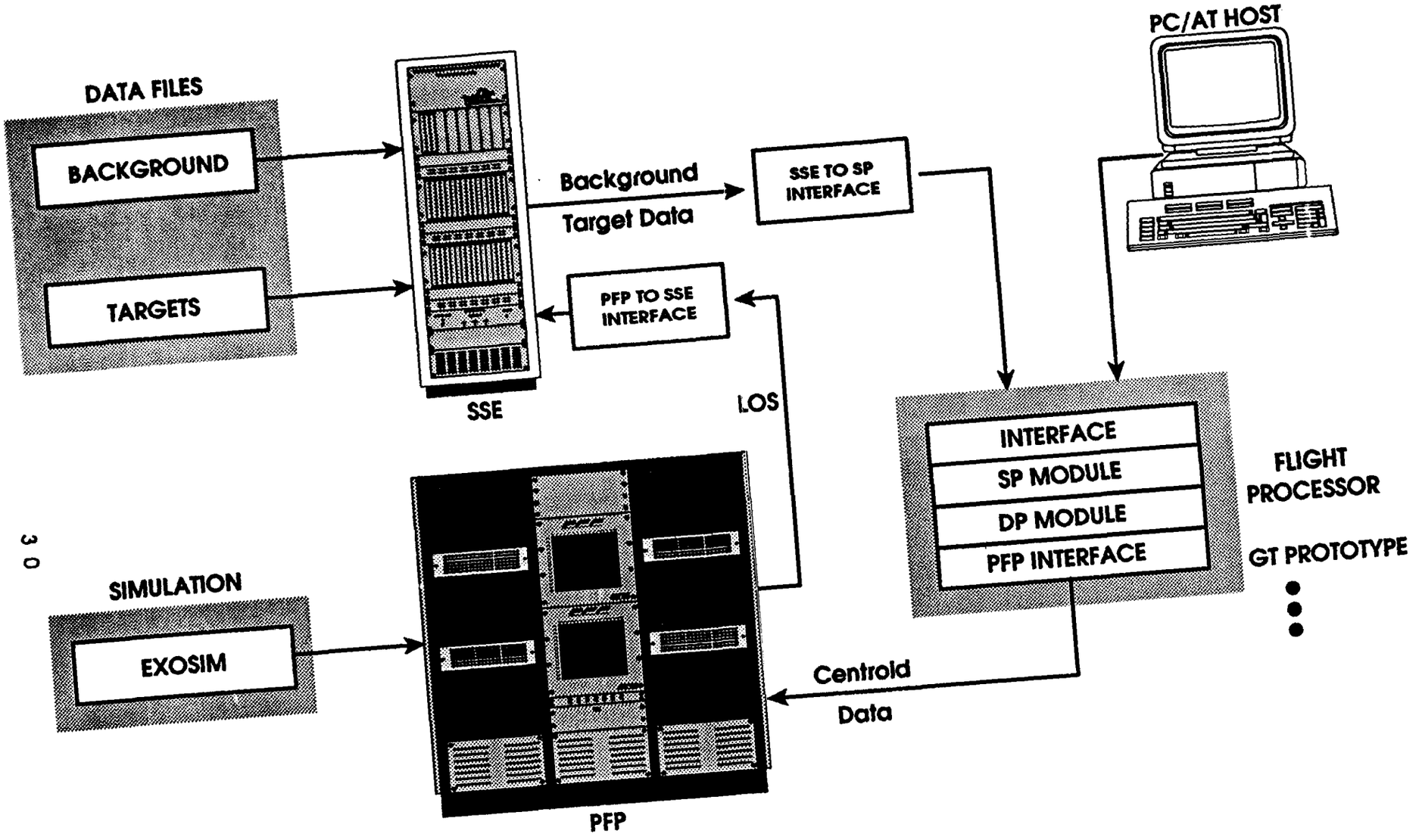


Figure 3.5
DETL Configureation for the EXOSIM Closed Loop Demonstration

E\G\P\H/GNCPRVAL

5.1.2 GBI/LEAP/E^2I

GBI, LEAP, and E^2I are all examples of programs that the PFP and DETL facility are equipped to support. Using the EXOSIM work and partitioning experience as a starting point, real time parallel simulations for any of these programs could be developed. The initial partitioning could be developed at Georgia Tech and then shipped to the KDEC facility, where KDEC personnel and contractors could use these programs for analysis, modify and refine them, and gradually move into the parallel simulation/emulation field.

5.2 Planned Developments

The emphasis for this reporting period has been in developing applications to run on the PFP, and in the design and integration of the GN&C processor. The knowledge and experience gained through working these phases of the program has added new insight that can be translated into improvements for the PFP system. Since the system architecture is very modular, the improvements can be made in incremental steps so that the system never becomes completely outdated and the system components and software are used for their full life span.

5.2.1 New Crossbar

The objectives of a new crossbar are to increase the transfer speed, increase the number of ports on a single crossbar, and decrease the size of the unit. Two alternatives are under study, with preliminary designs under way on each. The first plan is to build the new crossbar so that it still requires a master state machine like the such as the sequencer. The second plan is to build the new crossbar that is dynamically reconfigurable so that the need for the master sequencer is eliminated.

Several implementation alternatives have been examined for the crossbar that still requires a separate sequencer. A literature search on the commercially available crossbar switch chips has been undertaken, including several GaAs components. Many of the silicon based components are quoting very fast transfer rates once the part has been configured, but the time required to load the next configuration into the part and switch the connections restricts the applicability of these. In effect, it takes much longer to load the next configuration set up into the chip than it does to carry out most transfers. A custom designed 64 port non blocking VLSI crossbar chip appears to have the advantage over all of these because the configuration time is much less, since the chip has been designed to load much of the configuration information in parallel. This chip is presently the first choice for implementation. The GaAs based components are extremely fast, but are also extremely expensive, the available parts selection is still very limited, they are mostly available in suface mount components with non-standard pin spacings, they run from voltages that are not always consistent with TTL levels, and often are not consistent with GaAs voltage levels from different manufacturers.

The sequencer-less implementation is based on Inmos' new C104 switch. This chip contains an on chip dynamic routing strategy for sending messages. While the elimination of the sequencer simplifies the hardware, the software overhead is increased. Each message is divided into 32 byte packets and each packet must have a header on it specifying destination information.

If the data transferred between processors is very long, then this overhead information appears minimal. However, if the message is only several words, then the overhead information can dominate, so that the actual transfer time is much longer than the quoted peak rates. Since the implementation of this alternative is very straightforward, a prototype implementation is currently in the design process.

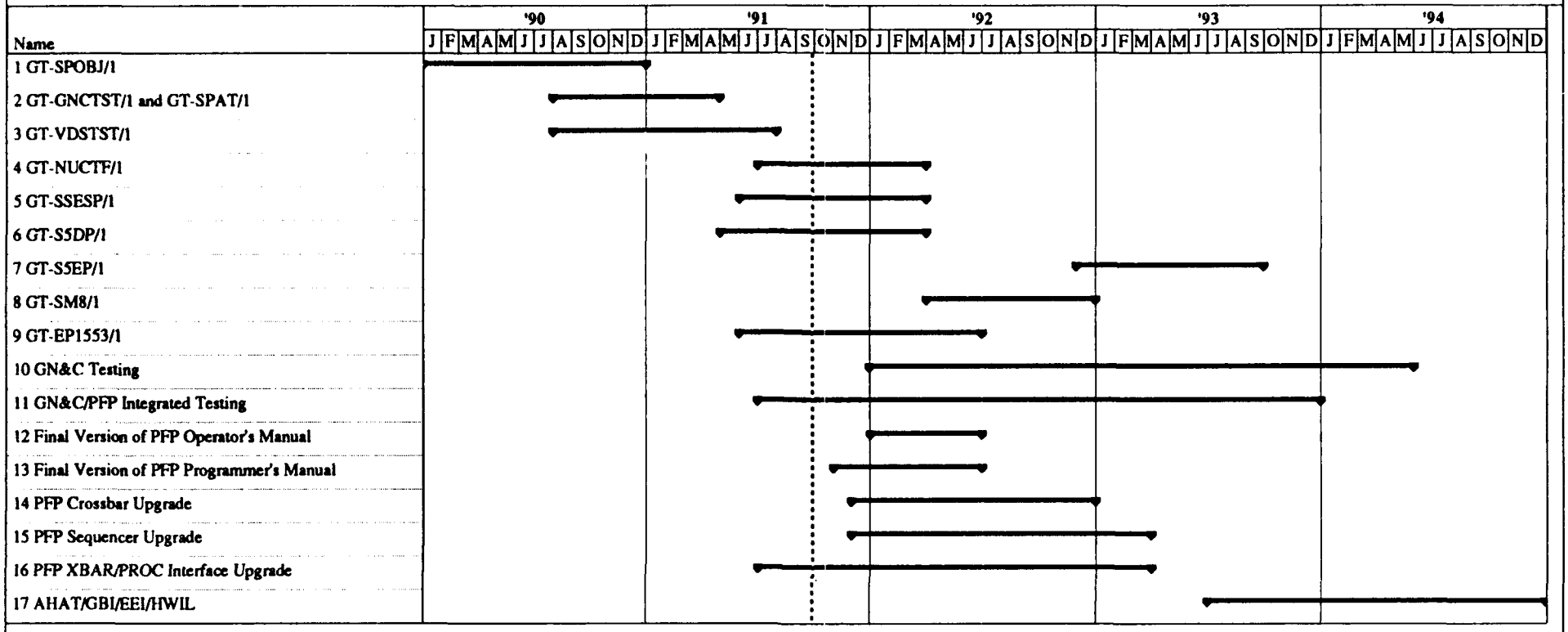
5.2.2 New Sequencer

Desired improvements in the current sequencer include increased speed, support for interrupts from the processor array, looping and branching capability within the sequencer code, support for variable length data transfers, and increased degugging capability including a single step mode. A new design incorporating these features is currently under way. The objective of this next version will be to build a sequencer that is a plug in replacement for the existing sequencer, but contains these added features. Some features, such as interrupt capability from a processor, must also be implemented at the processor end. New processor work is also under development, so that the newer processors would be able to take advantage of this feature.

5.2.3 New Processor/Crossbar Interface

The current PFP system has been able to support a number of commercially available processors which contain the Intel standard iSBX port. Several versions of a crossbar interface that plug on to an iSBX connector have been built, and are currently in use. In order to take full advantage of the increased crossbar and sequencer features that have been discussed, new standard interfaces will also be designed. In addition, a standard Multibus base board capable of accepting processor modules is also in development. This approach is described in Volume X of this report.

Figure 6.1. Schedule for GNC Development and PFP Integration



7. References

1. Woods, M, Parallel Function Processor Hardware Operation, *Computer Engineering Research Laboratory Special Technical Report*, STR-0142-90-005.2, Georgia Institute of Technology, submitted to the United States Army Strategic Defense Command for contract DASG60-89-C-0142, (March 1991).

2. Collins, Thomas R., et al, *Computer Engineering Research Laboratory Final Technical Report*, Volume 1, Georgia Institute of Technology, submitted to the United States Army Strategic Defense Command for contract No. DASG60-85-C-0041, (July 1989).

3. Woods, M., Pitts, R., and Bingham, P., Parallel Function Processor Development, *Computer Engineering Research Laboratory Annual Report*, Volume 4, Georgia Institute of Technology, submitted to the United States Army Strategic Defense Command for contract DASG60-89-C-0142, (August 1990).

4. Woods, M, et. al., Parallel Function Processor Technical Data Package, *Computer Engineering Research Laboratory*, Georgia Institute of Technology, submitted to the United States Army Strategic Defense Command for contract DASG60-89-C-0142, (March 1990).

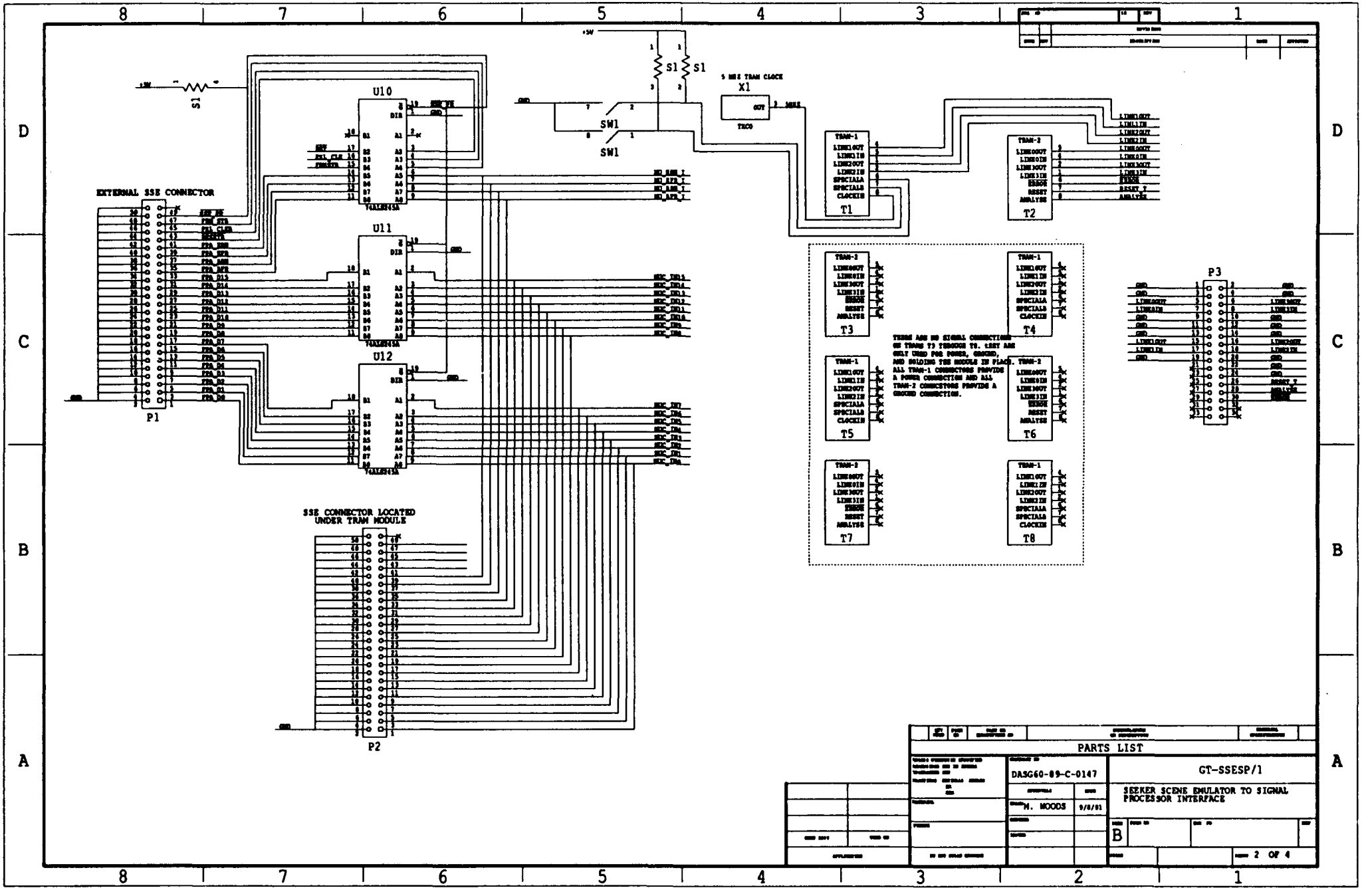
5. Pitts, R., Parallel Function Processor Programmer's Manual, *Computer Engineering Research Laboratory Special Technical Report*, STR-0142-90-006.1, Georgia Institute of Technology, submitted to the United States Army Strategic Defense Command for contract DASG60-89-C-0142, (May 1990).

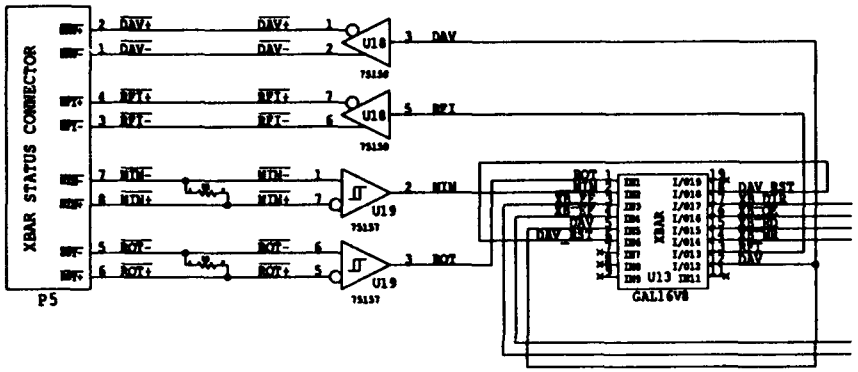
6. Alford, C., Abler, R., Register, A., and Tan, W., Hardware in the Loop Testing of KEW Flight Processors, *Proceedings of the 1990 Summer Computer Simulation Conference*, Calgary, Alberta, Canada, (July 1990), pp. 938-943.

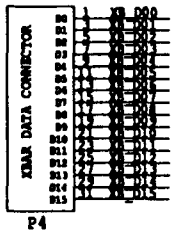
8. Appendix A: Schematics

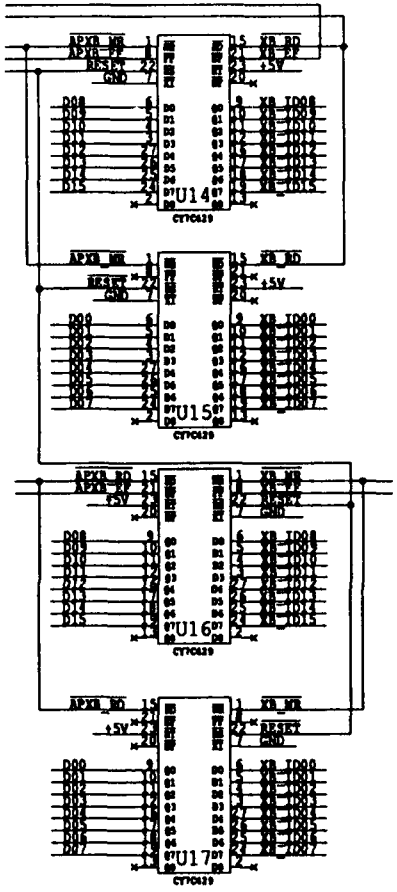
GT-SSESP/1 SCHEMATICS

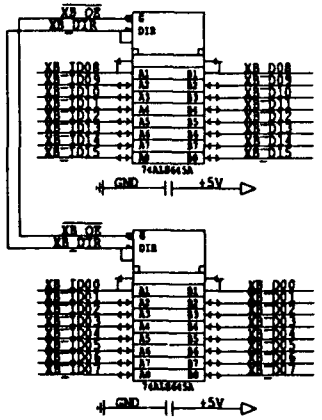

J1
+5V
GND
+5V
GND
+5V
GND
EADR_0
EADR_1
EADR_2
EADR_3
EADR_4
EADR_5
EADR_6
EADR_7
EADR_8
EADR_9
EADR_10
EADR_11
EADR_12
EADR_13
EADR_14
EADR_15
EADR_16
EADR_17
EADR_18
EADR_19
EADR_20
EADR_21
+5V
GND
+5V
GND
+5V
GND
EADR_22
EADR_23
EADR_24
EADR_25
DAV2
DAV3
INT_0
INT_1
INT_2
INT_3
INT_4
INT_5
INT_6
INT_7
INT_8
STATUS_0
STATUS_1
STATUS_2
STATUS_3
STATUS_4
READ2
READ3
RESET
IO6
+5V
GND
+5V
GND
+5V
J2
+5V
GND
+5V
GND
+5V
GND
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
DATA_16
DATA_17
DATA_18
DATA_19
DATA_20
DATA_21
DATA_22
GND
+5V
GND
+5V
DATA_23
DATA_24
DATA_25
DATA_26
DATA_27
DATA_28
DATA_29
DATA_30
DATA_31
DS_0
DS_1
DS_2
DS_3
NCS2
NCS3
RFI2
RFI3
ODSSEL
IDSSEL
WRITE2
WRITE3
DR
GND
EST_CLKE
GND
PXL_CLKE
GND
+5V
GND
+5V
J3
+5V
GND
+5V
GND
+5V
GND
SF_IN0
SF_IN1
SF_IN2
SF_IN3
SF_IN4
SF_IN5
SF_IN6
SF_IN7
SF_IN8
SF_IN9
SF_IN10
SF_IN11
SF_IN12
SF_IN13
SF_IN14
SF_IN15
SF_BFR_I
SF_BRM_I
SF_EFR_I
SF_ERM_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLKS
GND
EST_CLKS
J4
+5V
GND
+5V
GND
+5V
GND
NUC_IN0
NUC_IN1
NUC_IN2
NUC_IN3
NUC_IN4
NUC_IN5
NUC_IN6
NUC_IN7
NUC_IN8
NUC_IN9
NUC_IN10
NUC_IN11
NUC_IN12
NUC_IN13
NUC_IN14
NUC_IN15
NU_BFR_I
NU_BRM_I
NU_EFR_I
NU_ERM_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLKS
GND
NUC_CLKS
GND
GND
GND
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
PARTS LIST
DASG60-89-C-0142
GT-SSESP/1
SEEKER SCENE EMULATOR TO SIGNAL PROCESSOR INTERFACE BOARD
M. WOODS
4/4/91
B
1 OF 4


EXTERNAL SSE CONNECTOR
P1
U10
U11
U12
SSE CONNECTOR LOCATED UNDER TRAM MODULE
P2
P3
SW1
X1
5 MHz TRAM CLOCK
T1
T2
T3
T4
T5
T6
T7
T8
THERE ARE NO SIGNAL CONNECTIONS ON TRAMS T3 THROUGH T8. THEY ARE ONLY USED FOR POWER, GROUND, AND HOLDING THE MODULE IN PLACE. ALL TRAM-1 CONNECTORS PROVIDE A POWER CONNECTION AND ALL TRAM-2 CONNECTORS PROVIDE A GROUND CONNECTION.
PARTS LIST
DASG60-09-C-0147
GT-SSESP/1
SEEKER SCENE EMULATOR TO SIGNAL PROCESSOR INTERFACE
M. WOODS
9/8/01
B
SHEET 2 OF 4



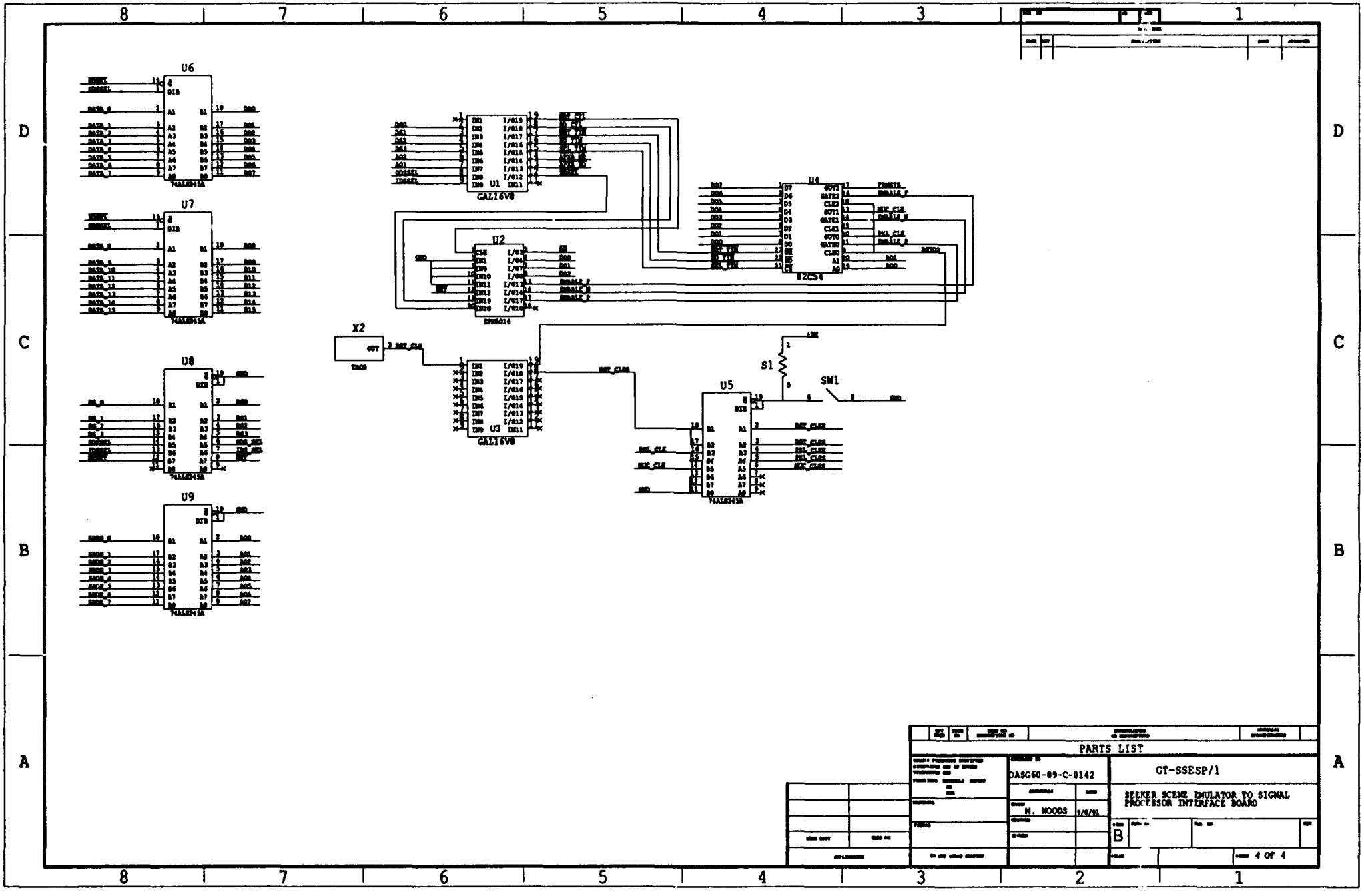






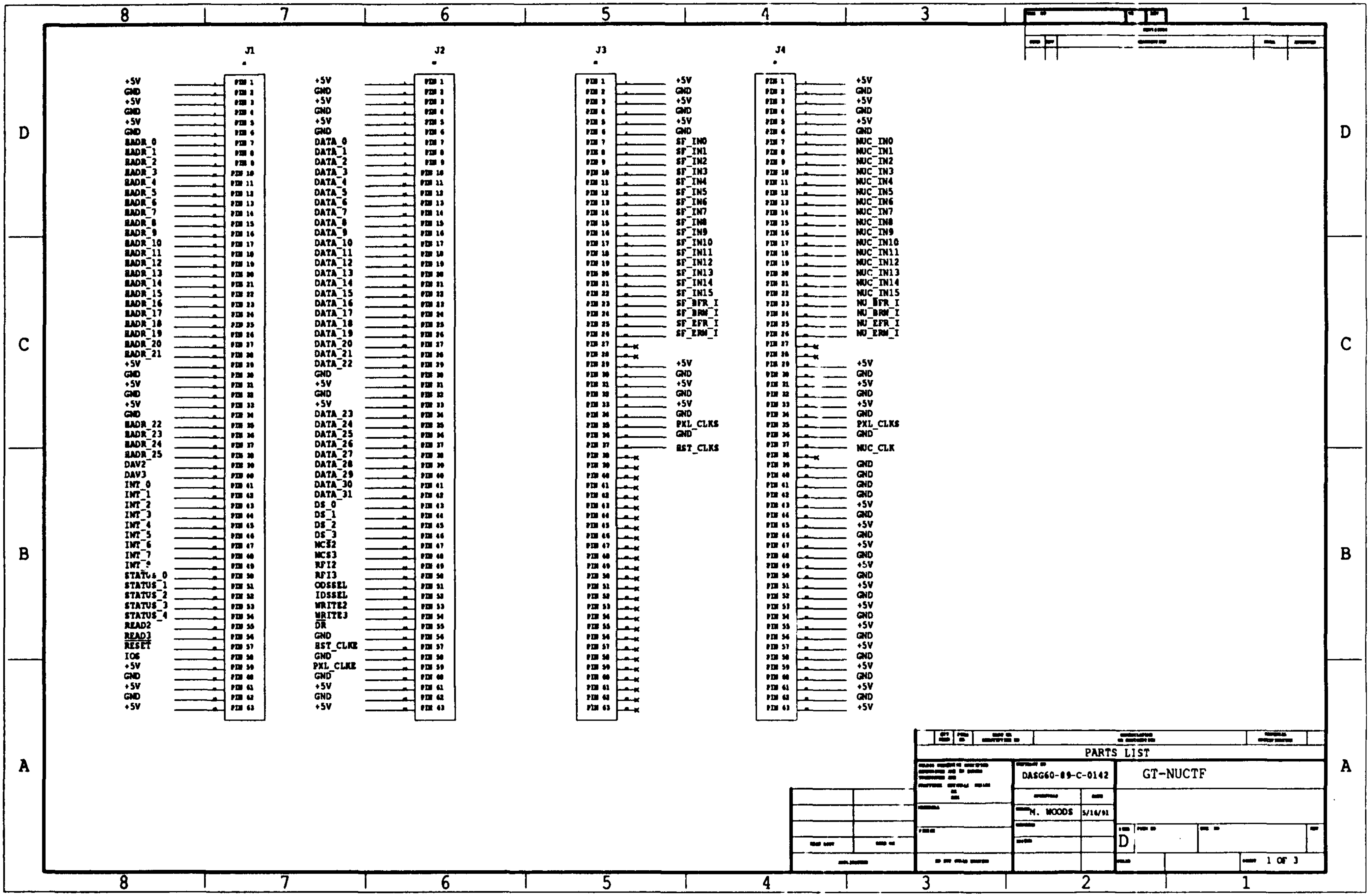
PARTS LIST

DASG60-89-C-0142	GT-SSESP/1
M. WOODS 9/8/91	SEEKER SCENE EMULATOR TO SIGNAL PROCESSOR INTERFACE BOARD
B	3 OF 4

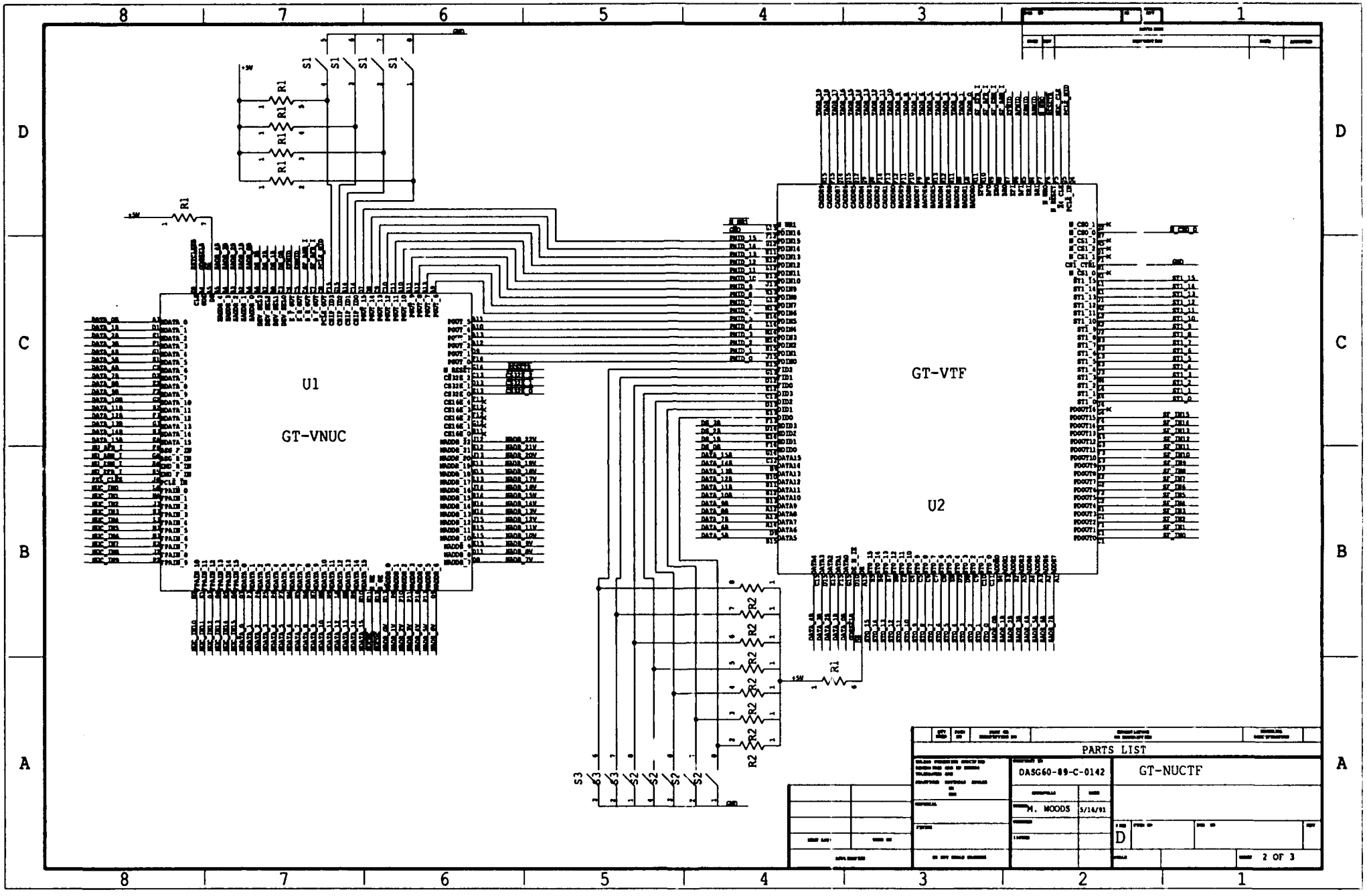

U6
U7
U8
U9
U1
GAL16V8
U2
82C54
U3
GAL16V8
U4
U5
X2
S1
SW1
PARTS LIST
DASG60-89-C-0142
GT-SSESP/1
SEEKER SCENE EMULATOR TO SIGNAL PROCESSOR INTERFACE BOARD
M. MOODS
9/8/91
B
4 OF 4

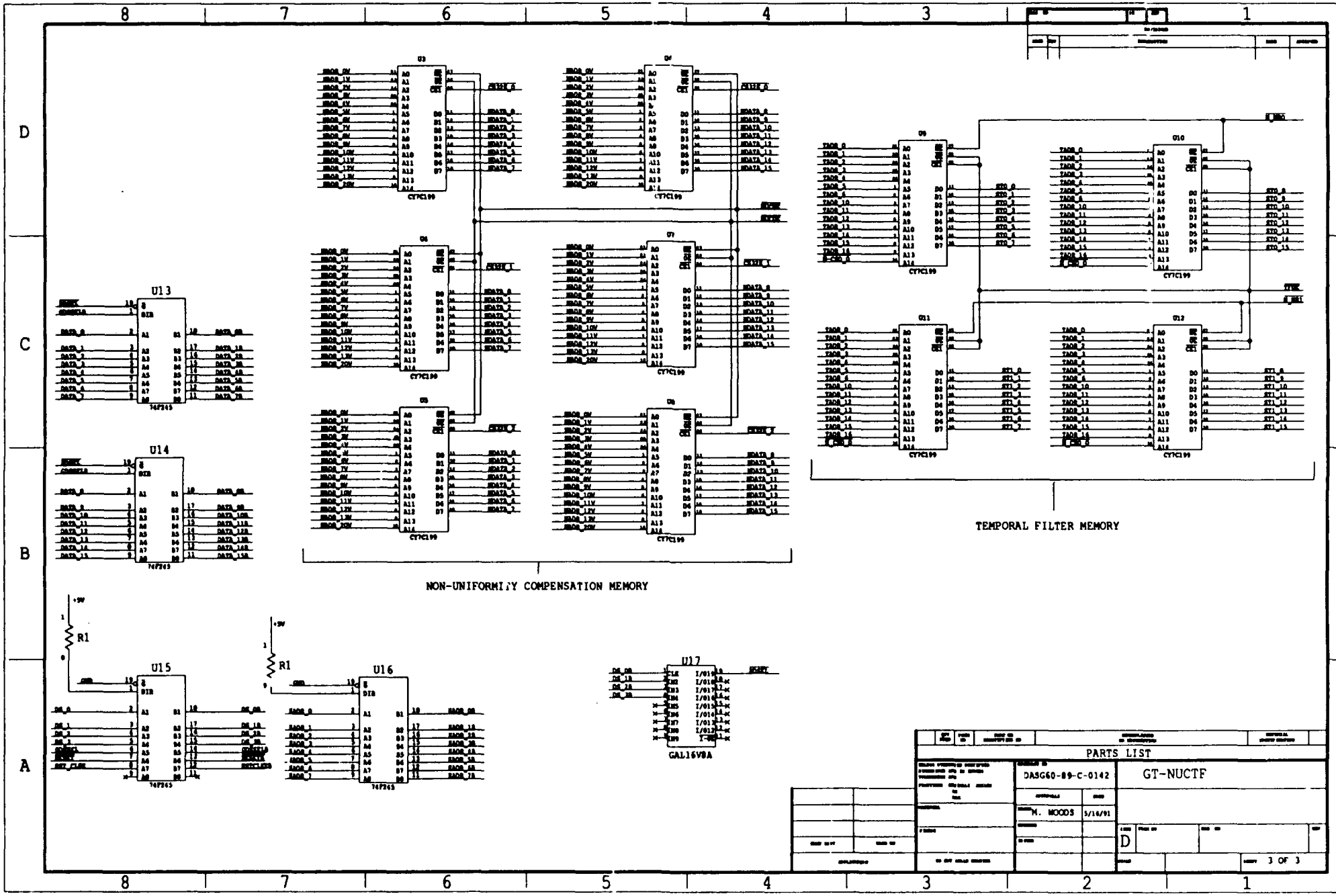
```
NAME     hostint;
Partno   000;
Date     09/16/91;
Revision 0.0;
Designer Dr. Michael B. Woods;
Company  Cerl, Georgia Tech;
Assembly GT-SSESP/1 Seeker Scene Emulator to Signal Processor Interface;
Location GAL3;
Device   G16V8;

/* Input */

Pin 1 = hst_clk;
Pin 2  = ds0;
Pin 3  = ds1;
Pin 4  = ds2;
Pin 5  = ds3;
Pin 6  = a2;
Pin 7  = a3;
Pin 8  = odssel;
Pin 9  = isdsel;

/* Output */

Pin 12 = bd_sel;
Pin 13 = !xb_rd;
Pin 14 = !xb_wrt;
Pin 15 = !tim_sel;
Pin 16 = !tim_rd;
Pin 17 = !tim_wrt;
Pin 18 = ctl_rd;
Pin 19 = ctl_wrt;

/* Intermediate Variable Definitions */
bdsel    (!ds0 & !ds1 & ds2 & ds3)

/* Logic Equations */

bd_sel   = bdsel;
xb_rd    = bdsel & a3 & !a2 & !odssel & idssel;
xb_wrt   = bdsel & a3 & !a2 & odssel & !idssel;
tim_sel  = bdsel & !a3 & a2;
tim_rd   = bdsel & !a3 & a2 & !odssel & ids el;
tim_wrt  = bdsel & !a3 & a2 & odssel & !idssel;
ctl_rd   = bdsel & !a3 & !a2 & !odssel & idssel;
ctl_wrt  = bdsel & !a3 & !a2 & odssel & !idssel;
```

GT-NUCTF/1 SCHEMATICS

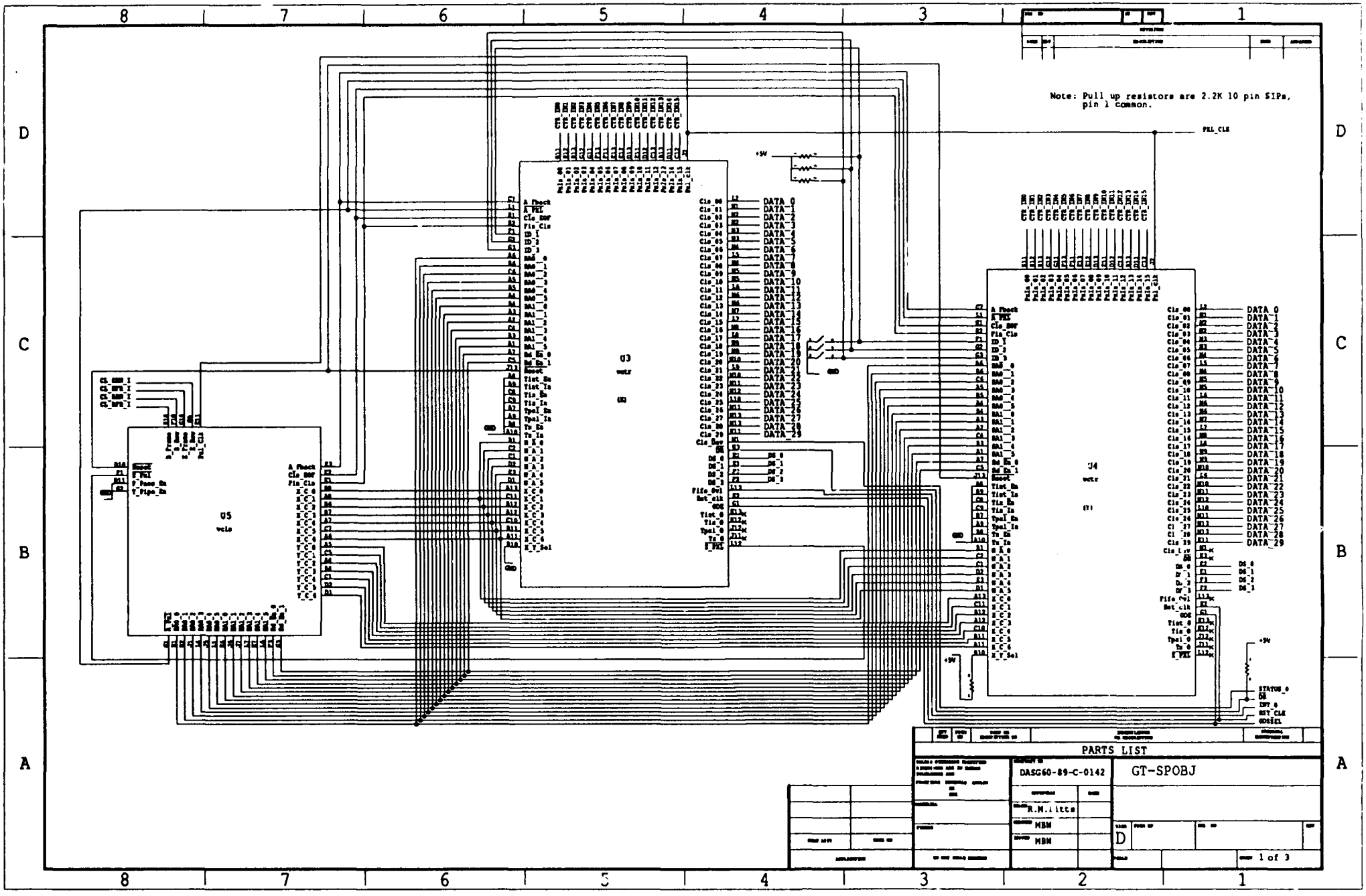


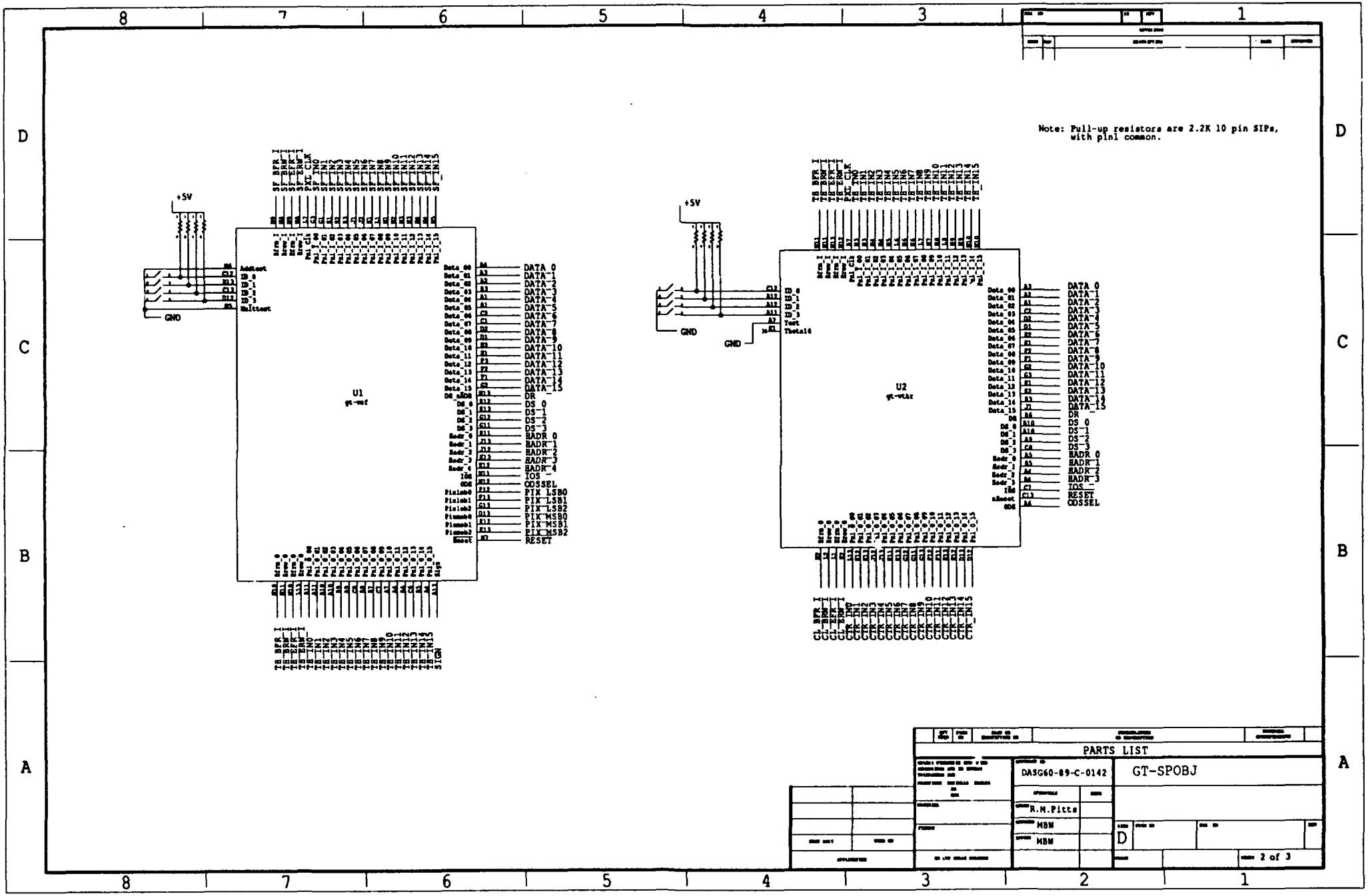
8 7 6 5 4 3 2 1
D C B A
J1
+5V GND +5V GND +5V GND
BADR_0 BADR_1 BADR_2 BADR_3 BADR_4 BADR_5 BADR_6 BADR_7 BADR_8 BADR_9 BADR_10 BADR_11 BADR_12 BADR_13 BADR_14 BADR_15 BADR_16 BADR_17 BADR_18 BADR_19 BADR_20 BADR_21
+5V GND +5V GND +5V GND
BADR_22 BADR_23 BADR_24 BADR_25
DAV2 DAV3
INT_0 INT_1 INT_2 INT_3 INT_4 INT_5 INT_6 INT_7
STATUS_0 STATUS_1 STATUS_2 STATUS_3 STATUS_4
READ2 READ3 RESET IO6
+5V GND +5V GND +5V
J2
+5V GND +5V GND +5V GND
DATA_0 DATA_1 DATA_2 DATA_3 DATA_4 DATA_5 DATA_6 DATA_7 DATA_8 DATA_9 DATA_10 DATA_11 DATA_12 DATA_13 DATA_14 DATA_15 DATA_16 DATA_17 DATA_18 DATA_19 DATA_20 DATA_21 DATA_22
GND +5V GND +5V
DATA_23 DATA_24 DATA_25 DATA_26 DATA_27 DATA_28 DATA_29 DATA_30 DATA_31
DS_0 DS_1 DS_2 DS_3
NCS2 NCS3 RFI2 RFI3 ODSSEL IDSSEL WRITE2 WRITE3 DR
GND RST_CLKE GND PXL_CLKE GND +5V GND +5V
J3
+5V GND +5V GND +5V GND
SF_IN0 SF_IN1 SF_IN2 SF_IN3 SF_IN4 SF_IN5 SF_IN6 SF_IN7 SF_IN8 SF_IN9 SF_IN10 SF_IN11 SF_IN12 SF_IN13 SF_IN14 SF_IN15
SF_BFR_I SF_BRM_I SF_EFR_I SF_ERM_I
+5V GND +5V GND +5V GND
PXL_CLKS GND RST_CLKS
J4
+5V GND +5V GND +5V GND
NUC_IN0 NUC_IN1 NUC_IN2 NUC_IN3 NUC_IN4 NUC_IN5 NUC_IN6 NUC_IN7 NUC_IN8 NUC_IN9 NUC_IN10 NUC_IN11 NUC_IN12 NUC_IN13 NUC_IN14 NUC_IN15
NU_BFR_I NU_BRM_I NU_EFR_I NU_ERM_I
+5V GND +5V GND +5V GND
PXL_CLKS GND NUC_CLK
GND GND GND GND +5V GND +5V GND +5V GND +5V GND +5V GND +5V GND +5V GND +5V GND +5V GND +5V GND +5V
PARTS LIST
DASG60-89-C-0142
GT-NUCTF
M. WOODS 5/16/91
D
1 OF 3


U1
GT-VNUC
GT-VTF
U2
PARTS LIST
DA5G60-89-C-0142
GT-NUCTF
M. WOODS
5/14/91
D
2 OF 3


NON-UNIFORMITY COMPENSATION MEMORY
TEMPORAL FILTER MEMORY
U13
U14
U15
U16
U17
R1
GAL16V8A
PARTS LIST
DASG60-89-C-0142
GT-NUCTF
M. WOODS
5/16/91
3 OF 3

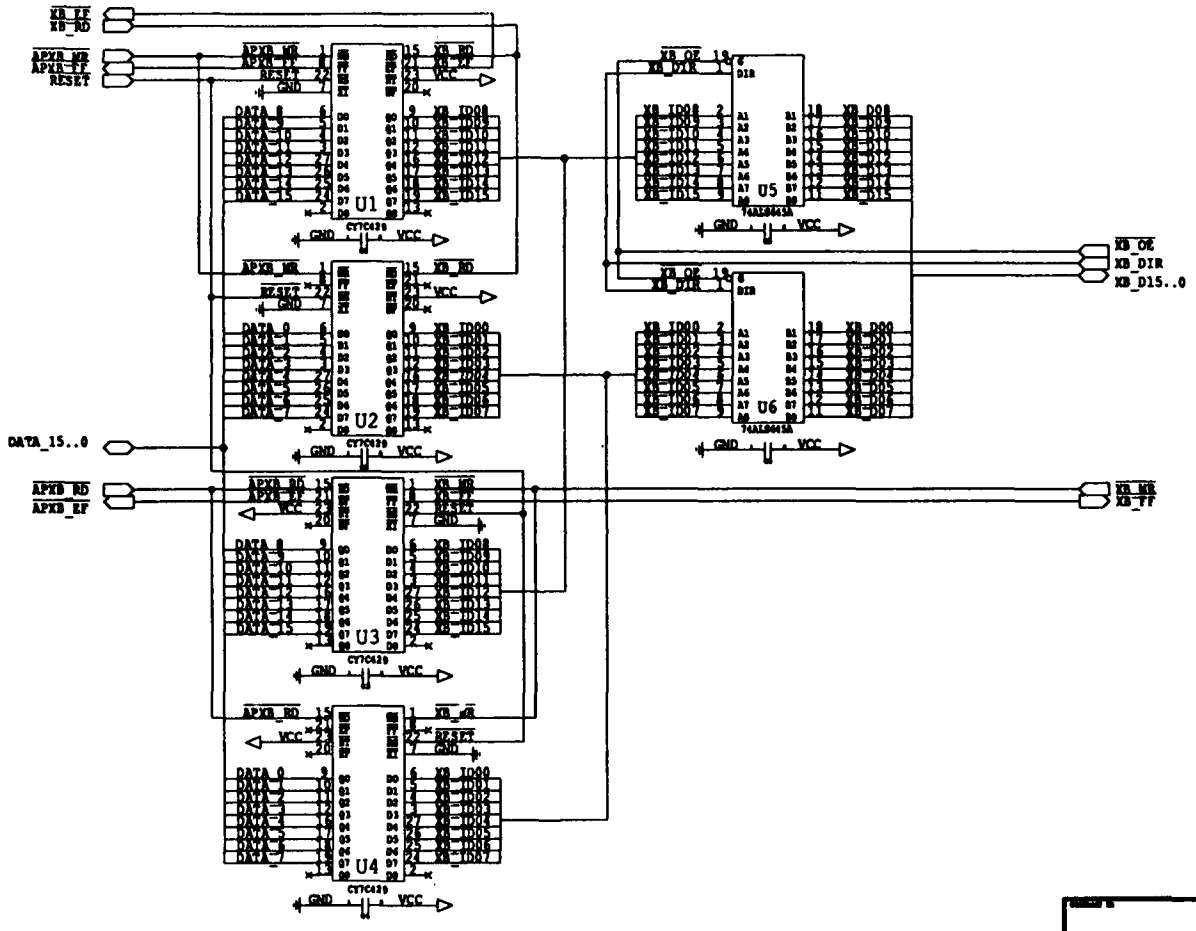
GT-SPOBJ/1 SCHEMATICS


Note: Pull up resistors are 2.2K 10 pin SIPs, pin 1 common.
PARTS LIST
DASG60-89-C-0142
GT-SPOBJ
R.M.Litts
MBN
MBN
1 of 3

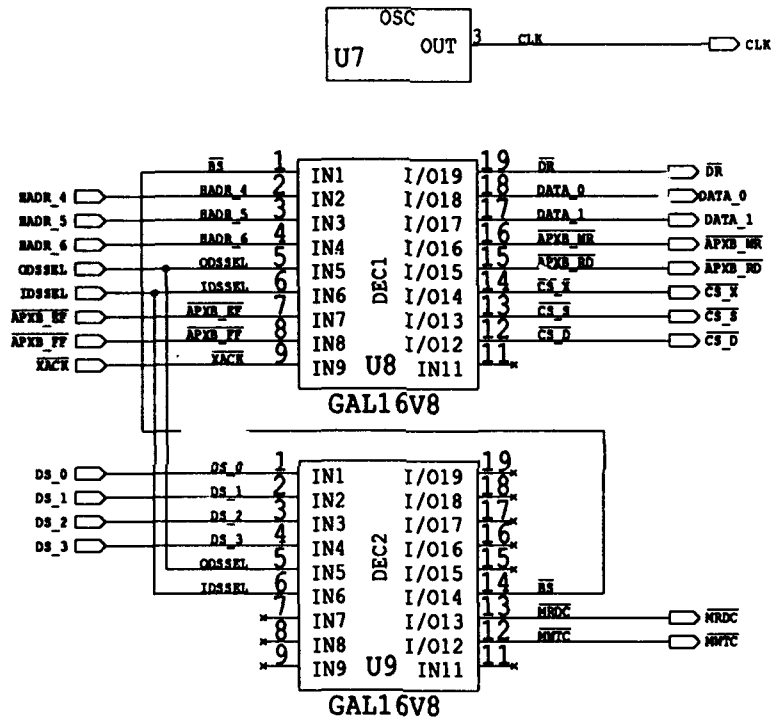

Note: Pull-up resistors are 2.2K 10 pin SIPs, with pin1 common.
+5V
GND
U1
gt-ref
U2
gt-vtxr
DATA 0
DATA-1
DATA-2
DATA-3
DATA-4
DATA-5
DATA-6
DATA-7
DATA-8
DATA-9
DATA-10
DATA-11
DATA-12
DATA-13
DATA-14
DATA-15
DR _
DS 0
DS-1
DS-2
DS-3
BADR 0
BADR-1
BADR-2
BADR-3
BADR-4
IOS _
CDSSEL
PIX LSB0
PIX-LSB1
PIX-LSB2
PIX-MSB0
PIX-MSB1
PIX-MSB2
RESET
PARTS LIST
DA5G60-89-C-0142
GT-SPOBJ
R.M.Pitts
MBW
MBW
D
2 of 3


J1
+5V
GND
+5V
GND
+5V
GND
BADR_0
BADR_1
BADR_2
BADR_3
BADR_4
BADR_5
BADR_6
BADR_7
BADR_8
BADR_9
BADR_10
BADR_11
BADR_12
BADR_13
BADR_14
BADR_15
BADR_16
BADR_17
BADR_18
BADR_19
BADR_20
BADR_21
+5V
GND
+5V
GND
+5V
GND
BADR_22
BADR_23
BADR_24
BADR_25
DAV2
DAV3
INT_0
INT_1
INT_2
INT_3
INT_4
INT_5
INT_6
INT_7
INT_8
STATUS_0
STATUS_1
STATUS_2
STATUS_3
STATUS_4
READ2
READ3
RESET
IOS
+5V
GND
+5V
GND
+5V
J2
+5V
GND
+5V
GND
+5V
GND
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
DATA_16
DATA_17
DATA_18
DATA_19
DATA_20
DATA_21
DATA_22
GND
+5V
GND
+5V
DATA_23
DATA_24
DATA_25
DATA_26
DATA_27
DATA_28
DATA_29
DATA_30
DATA_31
DS_0
DS_1
DS_2
DS_3
MCS2
MCS3
RFI2
RFI3
CDSSEL
IDSSEL
WRITE2
WRITE3
DR
GND
RST_CLK
GND
PXL_CLK
GND
+5V
GND
+5V
J3
+5V
GND
+5V
GND
+5V
GND
SF_IN0
SF_IN1
SF_IN2
SF_IN3
SF_IN4
SF_IN5
SF_IN6
SF_IN7
SF_IN8
SF_IN9
SF_IN10
SF_IN11
SF_IN12
SF_IN13
SF_IN14
SF_IN15
SF_BFR_I
SF_BRW_I
SF_EFR_I
SF_ERW_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLK
GND
J4
+5V
GND
+5V
GND
+5V
GND
NUC_IN0
NUC_IN1
NUC_IN2
NUC_IN3
NUC_IN4
NUC_IN5
NUC_IN6
NUC_IN7
NUC_IN8
NUC_IN9
NUC_IN10
NUC_IN11
NUC_IN12
NUC_IN13
NUC_IN14
NUC_IN15
NU_BFR_I
NU_BRW_I
NU_EFR_I
NU_ERW_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLK
GND
GND
GND
GND
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
PARTS LIST
DASG60-89-C-0142
SPOBJ
R.M.Pitts
MBW
MBW
D
3 of 3

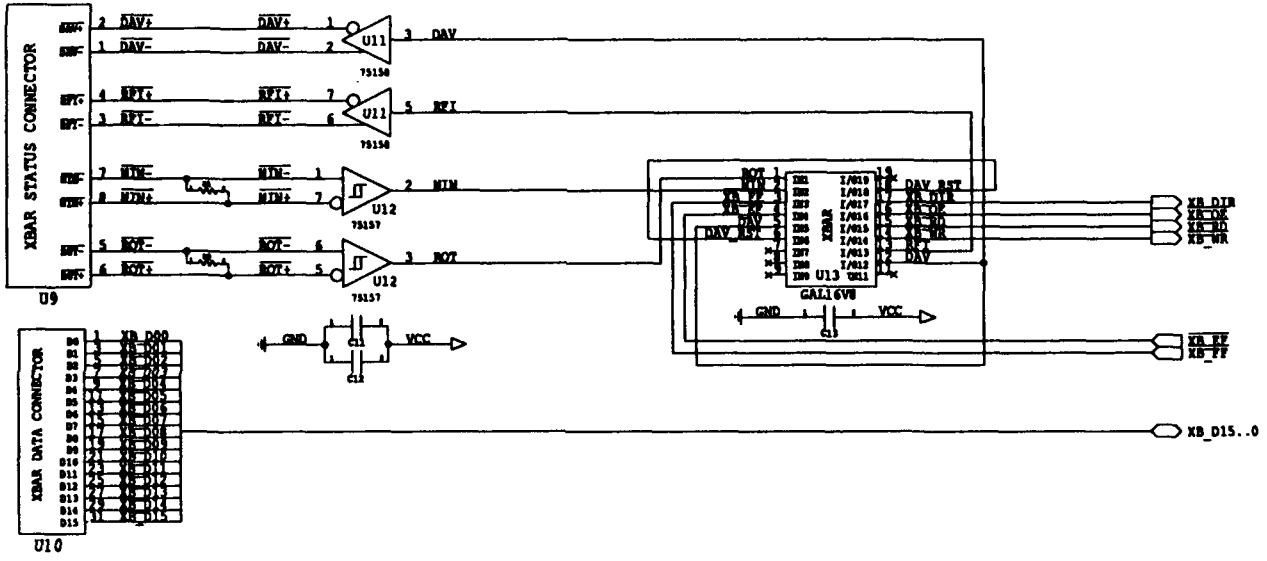
GT-S5DP/1 PROTOTYPE SCEMATICS



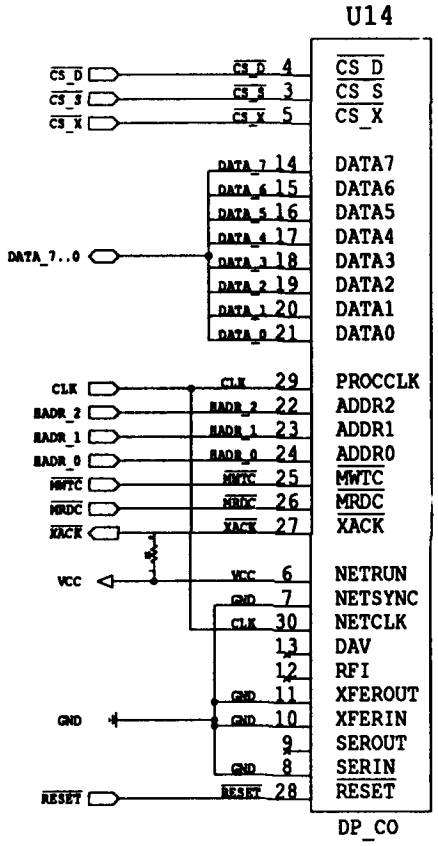
		Georgia Institute Of Technology Computer Engineering Research Lab
RLM	5-9-91	GT-DP/PFP Board
MST	5-9-91	*Crossbar FIFO Section*
		B
		NONE 1 of 5



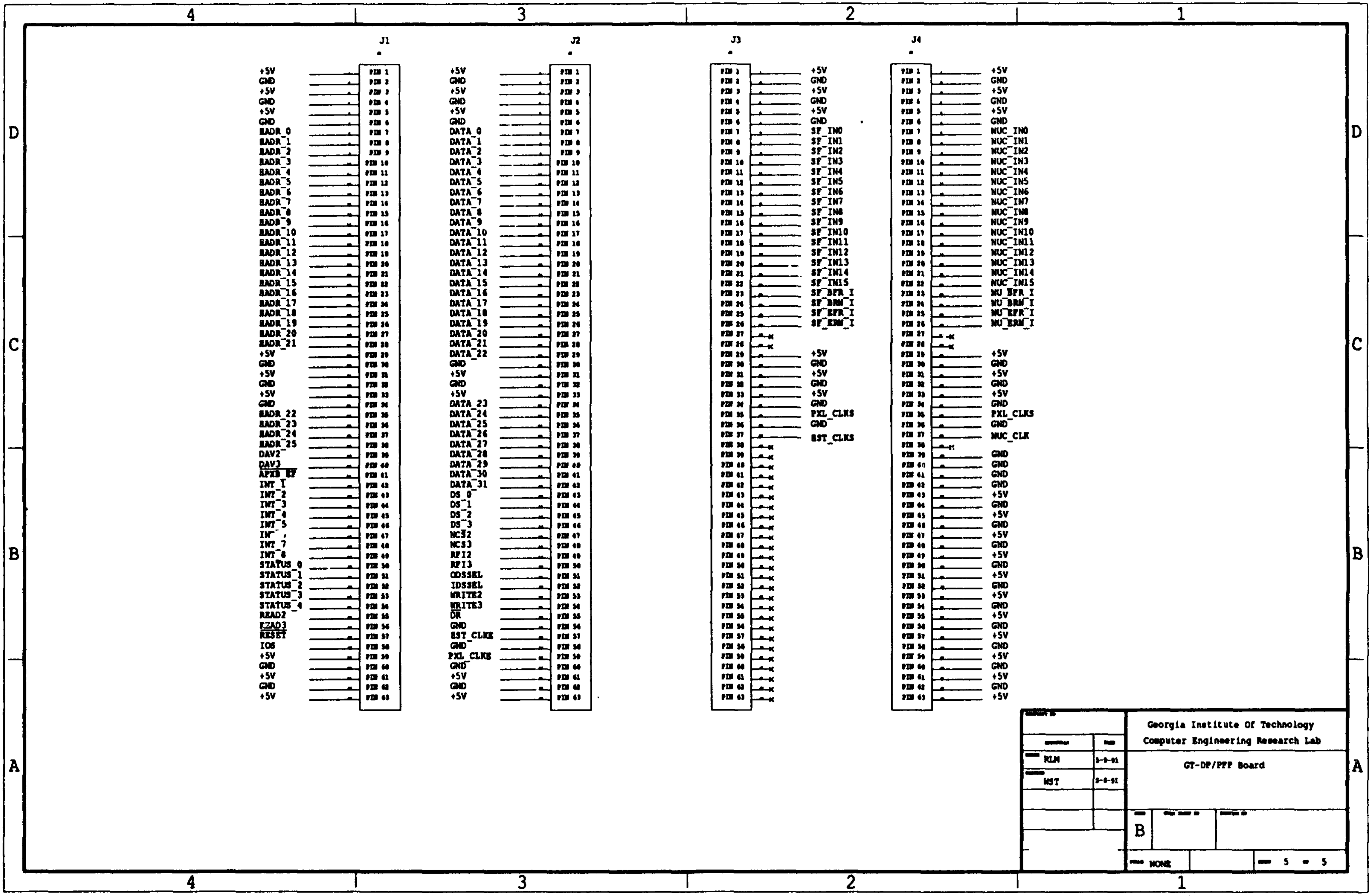
		Georgia Institute Of Technology Computer Engineering Research Lab
RLM	5-8-91	GT-DP/FFP Board Decoder Section
MST	5-8-91	
		B
		NONE 2 of 5



		Georgia Institute Of Technology
		Computer Engineering Research Lab
RLM	5-8-01	GT-DP/PFP Board
MST	5-8-01	Crossbar Connection Section
		B
		NONE 3 of 5



		Georgia Institute Of Technology Computer Engineering Research Lab
RLM	5-8-01	GT-DP/PFP Board Data Processor Connector
MST	5-8-01	
		B
		NONE 4 of 5


J1
+5V
GND
+5V
GND
+5V
GND
BADR_0
BADR_1
BADR_2
BADR_3
BADR_4
BADR_5
BADR_6
BADR_7
BADR_8
BADR_9
BADR_10
BADR_11
BADR_12
BADR_13
BADR_14
BADR_15
BADR_16
BADR_17
BADR_18
BADR_19
BADR_20
BADR_21
+5V
GND
+5V
GND
+5V
GND
BADR_22
BADR_23
BADR_24
BADR_25
DAV2
DAV3
APXB_EF
INT_1
INT_2
INT_3
INT_4
INT_5
INT_ ,
INT_7
INT_8
STATUS_0
STATUS_1
STATUS_2
STATUS_3
STATUS_4
READ2
EZAD3
RESET
IO6
+5V
GND
+5V
GND
+5V
J2
+5V
GND
+5V
GND
+5V
GND
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
DATA_16
DATA_17
DATA_18
DATA_19
DATA_20
DATA_21
DATA_22
GND
+5V
GND
+5V
DATA_23
DATA_24
DATA_25
DATA_26
DATA_27
DATA_28
DATA_29
DATA_30
DATA_31
DS_0
DS_1
DS_2
DS_3
NCS2
NCS3
RFI2
RFI3
ODSSEL
IDSSEL
WRITE2
WRITE3
DR
GND
EST_CLKE
GND
PXL_CLKE
GND
+5V
GND
+5V
J3
+5V
GND
+5V
GND
+5V
GND
SF_IN0
SF_IN1
SF_IN2
SF_IN3
SF_IN4
SF_IN5
SF_IN6
SF_IN7
SF_IN8
SF_IN9
SF_IN10
SF_IN11
SF_IN12
SF_IN13
SF_IN14
SF_IN15
SF_BFR_I
SF_BRM_I
SF_EFR_I
SF_ERM_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLKS
GND
EST_CLKS
J4
+5V
GND
+5V
GND
+5V
GND
NUC_IN0
NUC_IN1
NUC_IN2
NUC_IN3
NUC_IN4
NUC_IN5
NUC_IN6
NUC_IN7
NUC_IN8
NUC_IN9
NUC_IN10
NUC_IN11
NUC_IN12
NUC_IN13
NUC_IN14
NUC_IN15
NU_BFR_I
NU_BRM_I
NU_EFR_I
NU_ERM_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLKS
GND
NUC_CLK
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+5V
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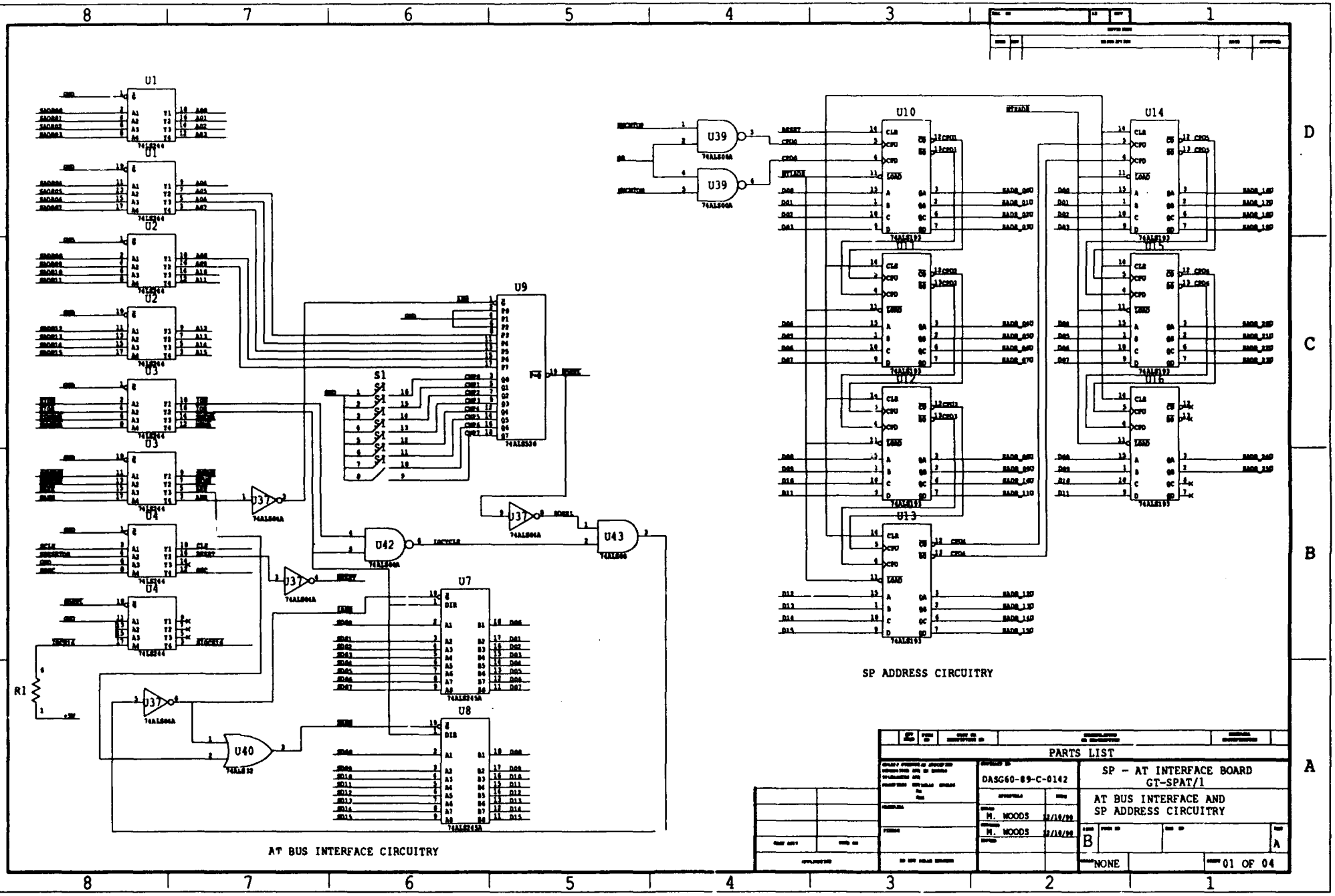
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
Georgia Institute Of Technology
Computer Engineering Research Lab
GT-DP/PFP Board
RLM 5-8-91
MST 5-8-91
B
NONE
5 of 5

```
NAME     dec1;
Partno   000;
Date     5/7/91;
Revision 0.00;
Designer Dr. Tan;
Company  Cerl;
Assembly GT-DP/PFP;
Location none;
Device   G16V8;

/* Allowable Target Device Types: GAL16V8 */

/* Inputs */

Pin 1 = !BS;
Pin 2 = HADR_4;
Pin 3 = HADR_5;
Pin 4 = HADR_6;
Pin 5 = ODSSEL;
Pin 6 = IDSSEL;
Pin 7 = !APXB_EF;
PIN 8 = !APXB_FF;
Pin 9 = !XACK;

/* Outputs */

Pin 12 = !CS_D;
Pin 13 = !CS_S;
Pin 14 = !CS_X;
Pin 15 = !APXB_RD;
PiN 16 = !APXB_WR;
Pin 17 = DATA_0;
Pin 18 = DATA_1;
Pin 19 = !DR;

/* Logic Equations */

CS_S = BS & !HADR_6 & !HADR_5 & !HADR_4;
CS_D = BS & !HADR_6 & !HADR_5 &  HADR_4;
CS_X = BS & !HADR_6 &  HADR_5 & !HADR_4;
APXB_RD = !ODSSEL &  IDSSEL & BS & !HADR_6 &  HADR_5 &  HADR_4;
APXB_WR =  ODSSEL & !IDSSEL & BS & !HADR_6 &  HADR_5 &  HADR_4;


DATA_1.OE = BS & !ODSSEL &  IDSSEL &  HADR_6 & !HADR_5 & !HADR_4;
DATA_1 = APXB_EF;
DATA_0.OE = BS & !ODSSEL &  IDSSEL &  HADR_6 & !HADR_5 & !HADR_4;
DATA_0 = APXB_FF;
DR.OE = BS;
DR = BS & (!HADR_6 & !HADR_5 # !HADR_6 & HADR_5 & !HADR_4) & XACK #
   BS & !HADR_6 &  HADR_5 &  HADR_4 #
   BS &  HADR_6 & !HADR_5 & !HADR_4;
```

```
NAME     dec2;
Partno   000;
Date     5/7/91;
Revision 0.00;
Designer Dr. Tan;
Company  Cerl;
Assembly GT-DP/PFP;
Location none;
Device   G16V8;

/* Allowable Target Device Types: GAL16V8 */

/* Inputs */

Pin 1 = DS_0;
Pin 2 = DS_1;
Pin 3 = DS_2;
Pin 4 = DS_3;
Pin 5 = ODSSEL;
Pin 6 = IDSSEL;

/* Outputs */

Pin 12 = !MWTC;
Pin 13 = !MRDC;
Pin 14 = !BS;


/* Logic Equations */

BS   = (DS_3 & DS_2 & !DS_1 & !DS_0);
MWTC =  ODSSEL & !IDSSEL;
MRDC = !ODSSEL & IDSSEL;@
```

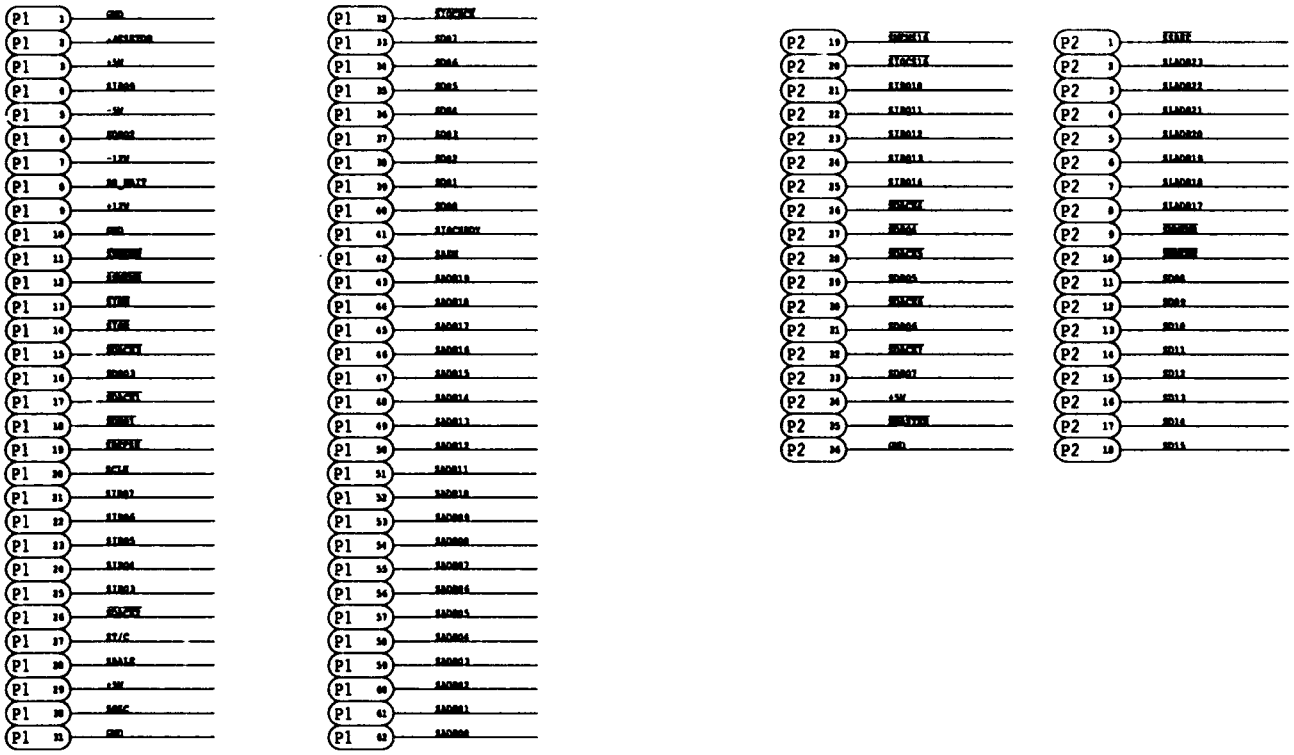
```
NAME     XBar;
Partno   000;
Date     9/11/90;
Revision 0.00;
Designer Dr. Tan;
Company  Cerl;
Assembly Multibus interface;
Location none;
Device   G16V8;

/* Allowable Target Device Types: GAL16V8 */

/* Inputs */

Pin 1 = ROT;
Pin 2 = WIN;
Pin 3 = !XB_FF;
Pin 4 = !XB_EF;
Pin 5 = DAV_IN;
Pin 6 = DAV_RST_IN;
Pin 7 = !reset;

/* Outputs */

Pin 12 = DAV;
Pin 13 = RFI;
Pin 14 = !XB_WR;
Pin 15 = !XB_RD;
Pin 16 = !XB_oe;
Pin 17 = XB_DIR;
Pin 18 = DAV_RST;

/* Logic Equations */

RFI   = !XB_FF;
XB_WR  = WIN;
XB_RD  = ROT & DAV_IN;
XB_DIR = ROT;
XB_oe  = (WIN # ROT);
DAV    = ROT & !reset & !XB_EF # !DAV_RST_IN;
DAV_RST = (!ROT # reset) # !DAV_IN;
```

GT-SPAT/1 SCHEMATICS



PARTS LIST

DASG60-89-C-0142	SP – AT INTERFACE BOARD GT-SPAT/1
M. WOODS 12/19/89	AT BUS INTERFACE AND SP ADDRESS CIRCUITRY
M. WOODS 12/19/89	B A
NONE	01 OF 04



PARTS LIST

DASG60-89-C-0142

SP - AT INTERFACE BOARD
GT-SPAT/1

AT BUS CONNECTOR PIN OUTS

M. WOODS 12/18/89

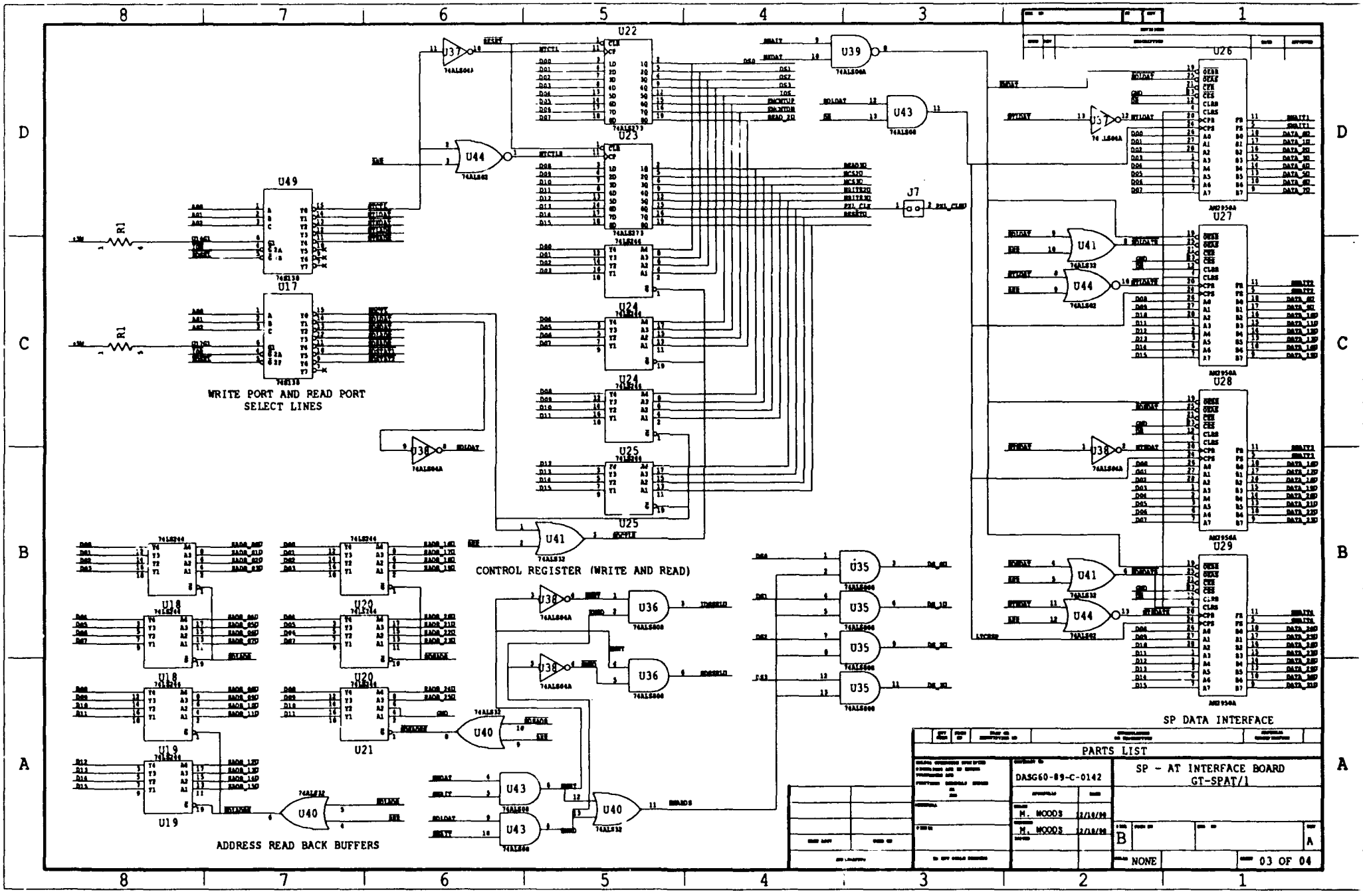
M. WOODS 12/18/89

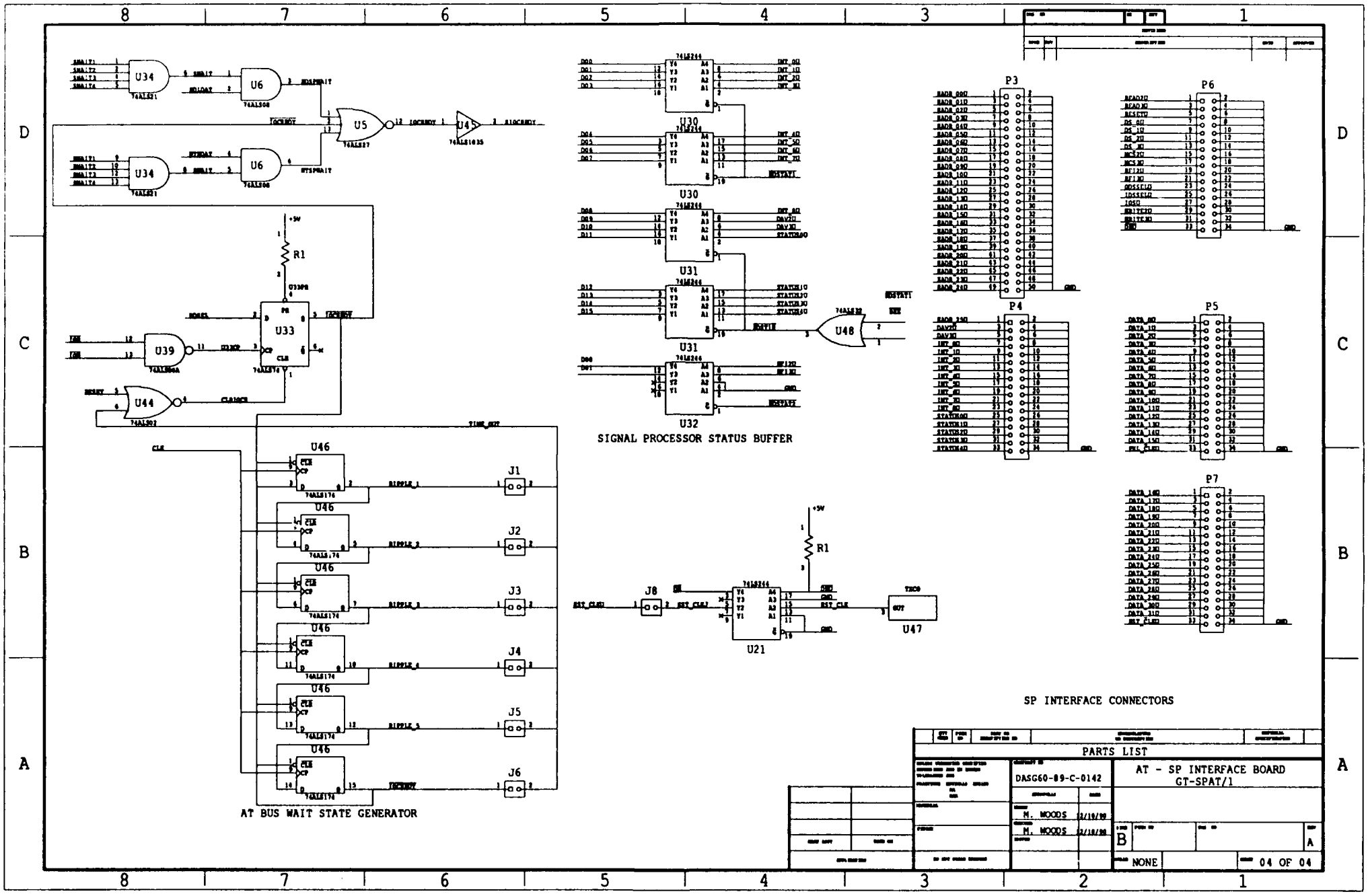
B

A

NONE

02 OF 04

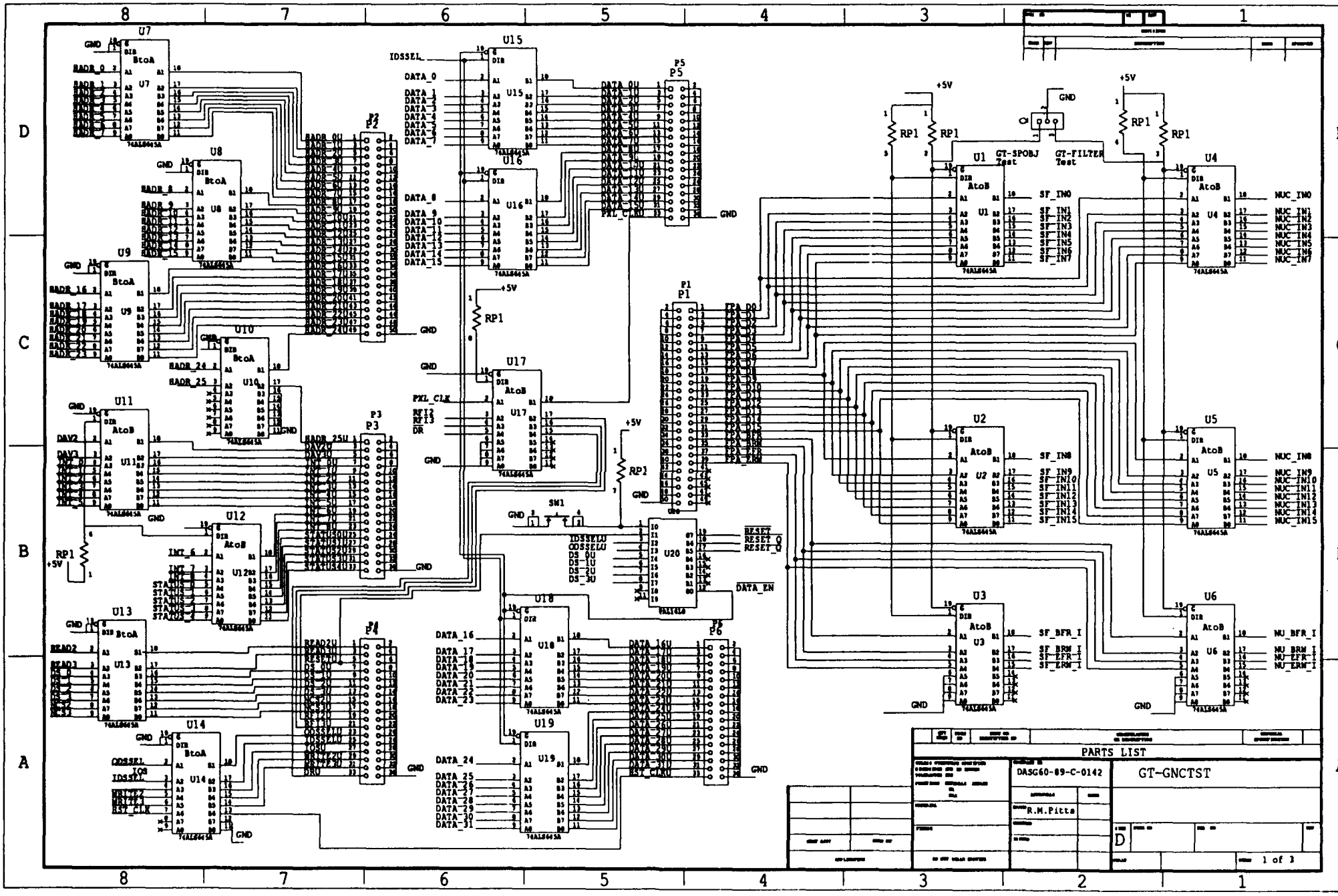

WRITE PORT AND READ PORT
SELECT LINES
CONTROL REGISTER (WRITE AND READ)
ADDRESS READ BACK BUFFERS
SP DATA INTERFACE
PARTS LIST
DASG60-89-C-0142
SP - AT INTERFACE BOARD
GT-SPAT/1
M. WOODS 12/19/89
M. WOODS 12/19/89
B
A
NONE
03 OF 04


U34
U6
U5
U4
U39
U44
U33
R1
U30
U31
U32
U48
SIGNAL PROCESSOR STATUS BUFFER
P3
P6
P4
P5
P7
U46
J1
J2
J3
J4
J5
J6
AT BUS WAIT STATE GENERATOR
J8
U21
U47
SP INTERFACE CONNECTORS
PARTS LIST
DASG60-89-C-0142
AT - SP INTERFACE BOARD
GT-SPAT/1
M. WOODS
NONE
04 OF 04

```
NAME     enb;
Partno   000;
Date     03/26/91;
Revision 0.0;
Designer Mike Woods;
Company  Cerl, Georgia Tech;
Assembly GT-SPAT Interface Board;
Location GAL3;
Device   G16V8;

/* Input */

/* Pin 1 = pxl_clk; */
Pin 2  = enwt;
Pin 3  = ds0;
Pin 4  = ds1;
Pin 5  = ds2;
Pin 6  = ds3;
Pin 7  = enrd;
Pin 8  = !dr;
Pin 9  = !reset;

/* Output */

Pin 12 = bus_en;
Pin 13 = !s0;
Pin 14 = !s1;
Pin 15 = !s2;
Pin 16 = wrck;
Pin 17 = rdck;
Pin 18 = !ios;
Pin 19 = !tr;


/* Logic Equations */
$DEFINE idle  'b'000
$DEFINE write0 'b'010
$DEFINE write1 'b'011
$DEFINE read0  'b'100
$DEFINE read1  'b'101
$DEFINE read2  'b'111
$DEFINE rsv0   'b'001
$DEFINE rsv1   'b'110

$DEFINE idles  (!s2 & !s1 & !s0)
$DEFINE write0s (!s2 &  s1 & !s0)
$DEFINE write1s (!s2 &  s1 &  s0)
$DEFINE read0s  ( s2 & !s1 & !s0)
$DEFINE read1s  ( s2 & !s1 &  s0)
$DEFINE read2s  ( s2 &  s1 &  s0)
```

```
$DEFINE rsv0s  (!s2 & !s1 &  s0)
$DEFINE rsv1s  ( s2 &  s1 & !s0)

$DEFINE thr ( ds3 & !ds2 & ds1 & !ds0)
$DEFINE sf  ( ds3 & !ds2 & ds1 &  ds0)
$DEFINE ctr (!ds3 & !ds2 & ds1)

bus_en = write0s # write1s # read0s # read1s # read2s # rsv0s # rsv1s;
wrck.d = write0s & dr;
rdck.d = read0s & (dr # ctr) & !sf # read2s & dr & sf;
tr    = read0s & dr # read1s & dr # read2s & dr # rsv0s & dr # rsv1s & dr
     # write0s & dr;
ios.d  = tr & !ios # !tr & ios # idles;

field state_machine = [s2..0];
SEQUENCE state_machine {
PRESENT idle    IF  ( enrd & !enwt & !reset) NEXT read0;
                IF  (!enrd &  enwt & !reset) NEXT write0;
           DEFAULT NEXT idle;
PRESENT write0  IF (dr # reset) NEXT idle;
                DEFAULT NEXT write0;
PRESENT write1  NEXT idle;
PRESENT read0   IF sf & dr & !reset NEXT read1;
           IF (ctr # (!sf)&dr # reset) NEXT idle;
                DEFAULT NEXT read0;
PRESENT read1   if (dr # reset) NEXT read2;
                DEFAULT NEXT read1;
PRESENT read2          if (dr # reset) NEXT idle;
           DEFAULT NEXT read2;
PRESENT rsv0           NEXT idle;
PRESENT rsv1  NEXT idle;
@
```

GT-GNCTST/1 SCHEMATICS


PARTS LIST
DASG60-89-C-0142
GT-GNCTST
R.M.Pitts
1 of 3


J1
+5V
GND
+5V
GND
+5V
GND
BADR_0
BADR_1
BADR_2
BADR_3
BADR_4
BADR_5
BADR_6
BADR_7
BADR_8
BADR_9
BADR_10
BADR_11
BADR_12
BADR_13
BADR_14
BADR_15
BADR_16
BADR_17
BADR_18
BADR_19
BADR_20
BADR_21
+5V
GND
+5V
GND
+5V
GND
BADR_22
BADR_23
BADR_24
BADR_25
DAV2
DAV3
INT_0
INT_1
INT_2
INT_3
INT_4
INT_5
INT_6
INT_7
INT_8
STATUS_0
STATUS_1
STATUS_2
STATUS_3
STATUS_4
READ2
READ3
RESET
IOS
+5V
GND
+5V
GND
+5V
J2
+5V
GND
+5V
GND
+5V
GND
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
DATA_16
DATA_17
DATA_18
DATA_19
DATA_20
DATA_21
DATA_22
GND
+5V
GND
+5V
DATA_23
DATA_24
DATA_25
DATA_26
DATA_27
DATA_28
DATA_29
DATA_30
DATA_31
DS_0
DS_1
DS_2
DS_3
NCS2
NCS3
RFI2
RFI3
ODSSEL
IDSSEL
WRITE2
WRITE3
DR
GND
BST_CLK
GND
PXL_CLK
GND
+5V
GND
+5V
J3
+5V
GND
+5V
GND
+5V
GND
SF_IN0
SF_IN1
SF_IN2
SF_IN3
SF_IN4
SF_IN5
SF_IN6
SF_IN7
SF_IN8
SF_IN9
SF_IN10
SF_IN11
SF_IN12
SF_IN13
SF_IN14
SF_IN15
SF_BFR_I
SF_BRM_I
SF_EFR_I
SF_ERM_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLK
GND
J4
+5V
GND
+5V
GND
+5V
GND
NUC_IN0
NUC_IN1
NUC_IN2
NUC_IN3
NUC_IN4
NUC_IN5
NUC_IN6
NUC_IN7
NUC_IN8
NUC_IN9
NUC_IN10
NUC_IN11
NUC_IN12
NUC_IN13
NUC_IN14
NUC_IN15
NU_BFR_I
NU_BRM_I
NU_EFR_I
NU_ERM_I
+5V
GND
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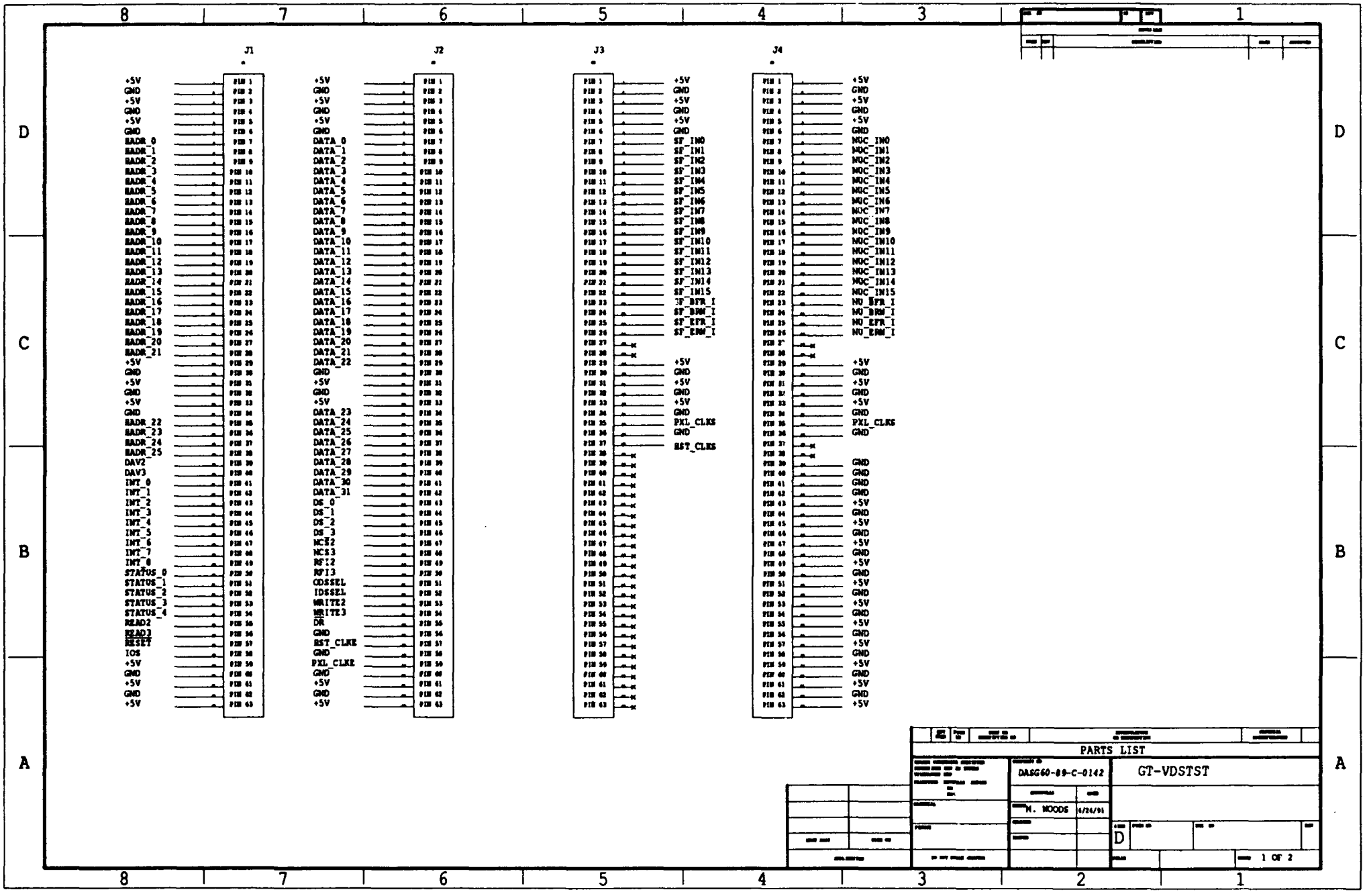
GND
PXL_CLK
GND
GND
GND
GND
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
GND
+5V
PARTS LIST
DASG60-89-C-0142
GT-GNCTST
R.M.Pitts
D
2 of 3


+5V
GND
ADR 0U
ADR 8U
ADR 16U
ADR 24U
INT 4U
DS 3U
WRITE2U
DATA 0U
DATA 8U
PXL CLKU
DATA 16U
DATA 24U
RST CLKU
FPA D0
FPA D8
FPA BFR
ADR 1U
ADR 9U
ADR 17U
ADR 25U
INT 5U
NCS2U
WRITE3U
DATA 1U
DATA 9U
DATA 17U
DATA 25U
FPA D1
FPA D9
FPA BRM
ADR 2U
ADR 10U
ADR 18U
DAV2U
INT 6U
READ2U
NCS3U
DRU
DATA 2U
DATA 10U
DATA 18U
DATA 26U
FPA D2
FPA D10
FPA EFR
ADR 3U
ADR 11U
ADR 19U
DAV3U
INT 7U
READ3U
RFI2U
DATA 3U
DATA 11U
DATA 19U
DATA 27U
FPA D3
FPA D11
FPA ERM
ADR 4U
ADR 12U
ADR 20U
INT 0U
INT 8U
RESETU
RFI3U
DATA 4U
DATA 12U
DATA 20U
DATA 28U
FPA D4
FPA D12
ADR 5U
ADR 13U
ADR 21U
INT 1U
DS 0U
IDSSELU
DATA 5U
DATA 13U
DATA 21U
DATA 29U
FPA D5
FPA D13
ADR 6U
ADR 14U
ADR 22U
INT 2U
DS 1U
IDSSELU
DATA 6U
DATA 14U
DATA 22U
DATA 30U
FPA D6
FPA D14
ADR 7U
ADR 15U
ADR 23U
INT 3U
DS 2U
IOSU
DATA 7U
DATA 15U
DATA 23U
DATA 31U
FPA D7
FPA D15
PARTS LIST
DA5G60-89-C-0142
GT-GNCTST
R.M.Pitts
D
3 of 3

GT-VDSTST/1 SCEMATICS


J1
+5V
GND
+5V
GND
+5V
GND
HADR_0
HADR_1
HADR_2
HADR_3
HADR_4
HADR_5
HADR_6
HADR_7
HADR_8
HADR_9
HADR_10
HADR_11
HADR_12
HADR_13
HADR_14
HADR_15
HADR_16
HADR_17
HADR_18
HADR_19
HADR_20
HADR_21
+5V
GND
+5V
GND
+5V
GND
HADR_22
HADR_23
HADR_24
HADR_25
DAV2
DAV3
INT_0
INT_1
INT_2
INT_3
INT_4
INT_5
INT_6
INT_7
INT_8
STATUS_0
STATUS_1
STATUS_2
STATUS_3
STATUS_4
READ2
READ3
RESET
IOS
+5V
GND
+5V
GND
+5V
J2
+5V
GND
+5V
GND
+5V
GND
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
DATA_16
DATA_17
DATA_18
DATA_19
DATA_20
DATA_21
DATA_22
GND
+5V
GND
+5V
DATA_23
DATA_24
DATA_25
DATA_26
DATA_27
DATA_28
DATA_29
DATA_30
DATA_31
DS_0
DS_1
DS_2
DS_3
NCS2
NCS3
RFI2
RFI3
ODSSEL
IDSSEL
WRITE2
WRITE3
DR
GND
RST_CLKE
GND
PXL_CLKE
GND
+5V
GND
+5V
J3
+5V
GND
+5V
GND
+5V
GND
SF_IN0
SF_IN1
SF_IN2
SF_IN3
SF_IN4
SF_IN5
SF_IN6
SF_IN7
SF_IN8
SF_IN9
SF_IN10
SF_IN11
SF_IN12
SF_IN13
SF_IN14
SF_IN15
SF_BFR_I
SF_BRM_I
SF_EFR_I
SF_ERM_I
+5V
GND
+5V
GND
+5V
GND
PXL_CLKS
GND
RST_CLKS
J4
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GND
+5V
GND
+5V
GND
NOC_IN0
NOC_IN1
NOC_IN2
NOC_IN3
NOC_IN4
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NOC_IN6
NOC_IN7
NOC_IN8
NOC_IN9
NOC_IN10
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NOC_IN12
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NO_EFR_I
NO_ERM_I
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GND
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GND
+5V
GND
+5V
GND
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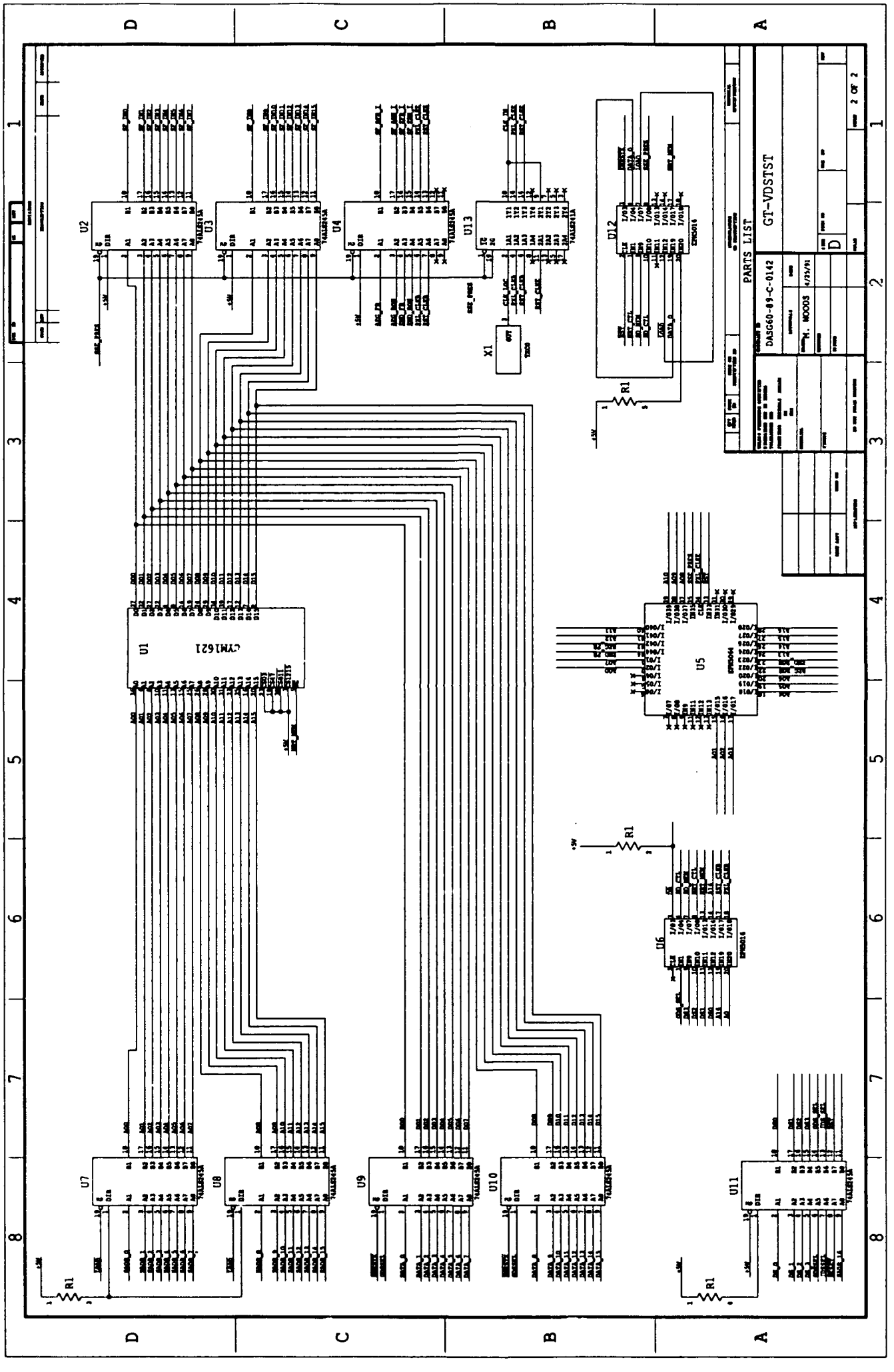
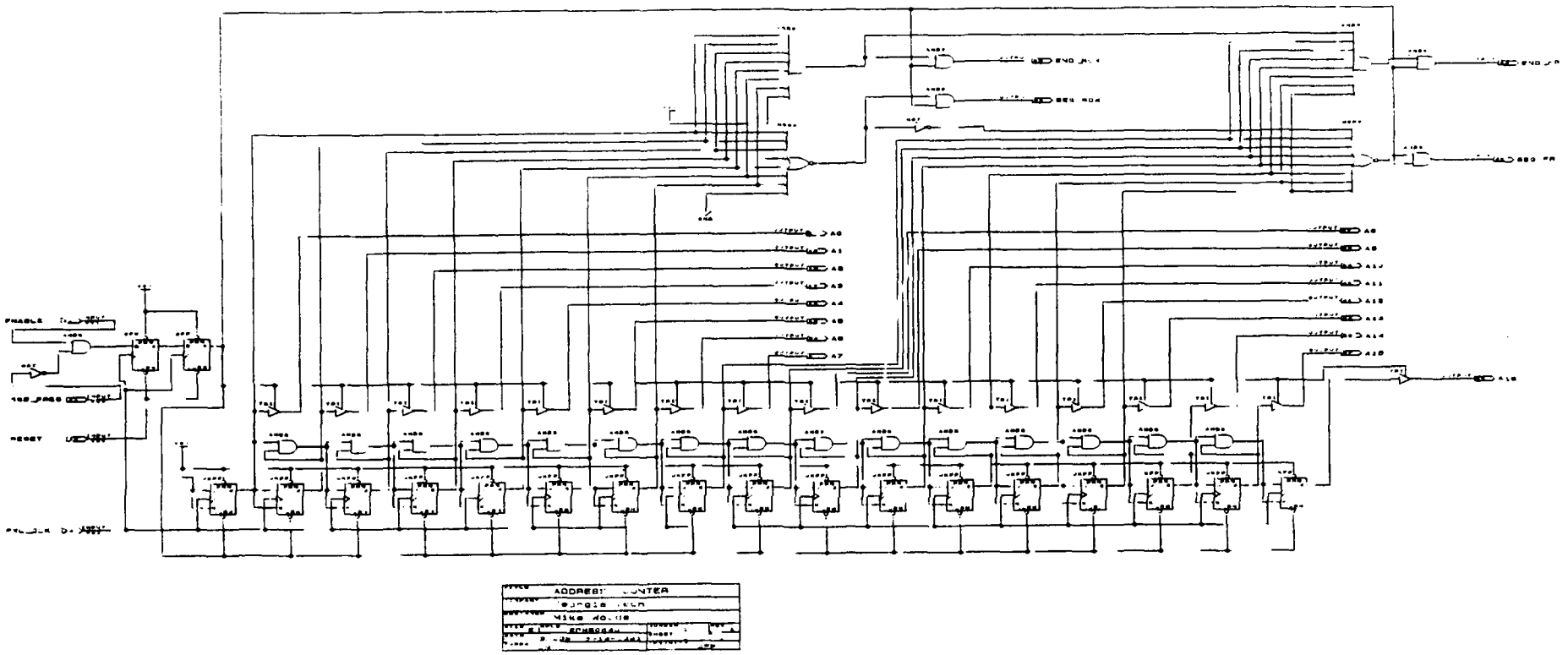
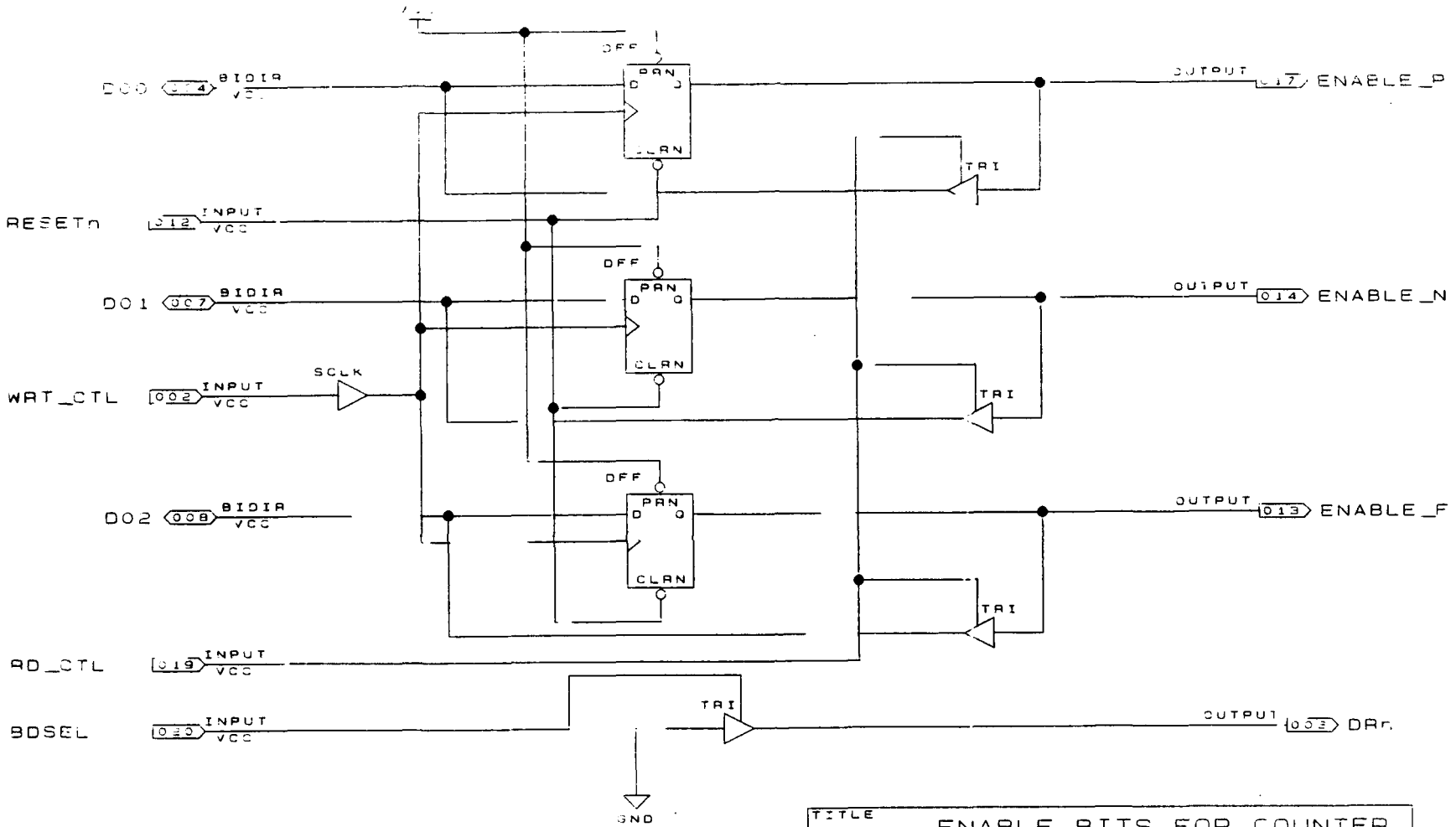
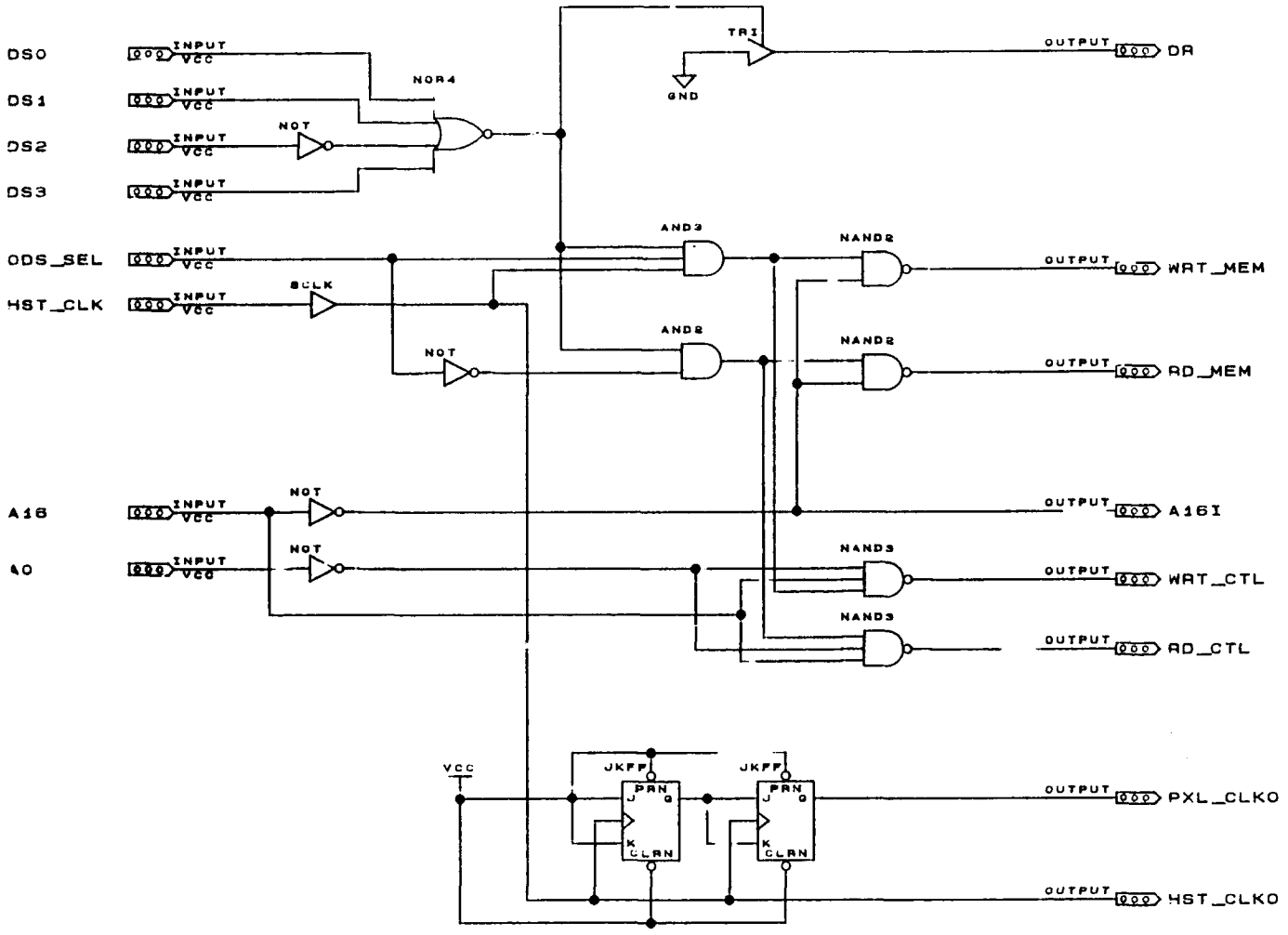
+5V
PARTS LIST
DASG60-89-C-0142
GT-VDSTST
M. WOODS 4/24/91
D
1 OF 2


PARTS LIST
GT-VDSTST
DAS660-89-C-0142
2 OF 2
U1
CYM1621
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
X1
R1

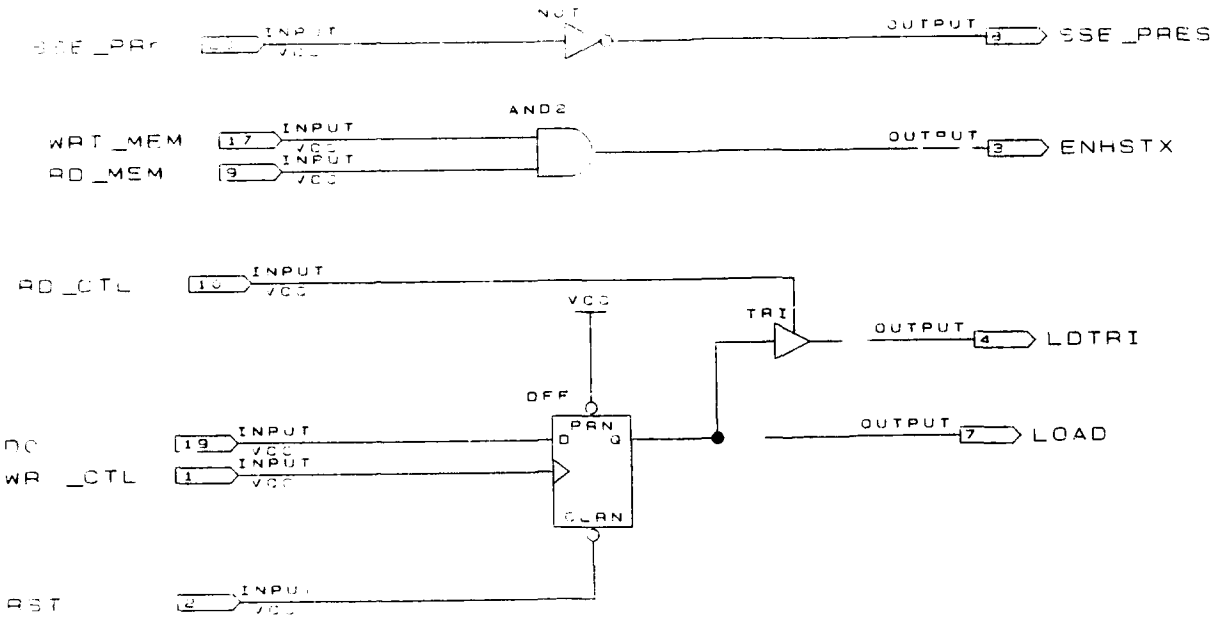

ADDRESS COUNTER
Wike 40.18
SCHEMA



TITLE	ENABLE BITS FOR COUNTER
COMPANY	Georgia Tech
DESIGNER	Mike Woods
SIZE B / EPLD EPM5016	NUMBER / REV A
DATE 9-16-19-1	SHEET 1 OF 1
TURBO N	RE DAT Y DFF



TITLE	EP BUS INTERFACE LOGIC		
COMPANY	Georgia Tech		
DESIGNER	Mike Woods		
SIZE D	EPLD EPM5016-1	NUMBER 1.00	REV A
DATE 11:01a 4-23-1991		SHEET 1 OF 1	
TURBO ON		SECURITY OFF	



TITLE	ENABLE EPLD
COMPANY	Georgia Tech
DESIGNED	Mike Woods
SIZE B EPLD EDME_1.0	NUMBER 1 REV A
DATE 3 Apr 94-3-1994	SHEET 1 OF 1
APP N	SECURITY